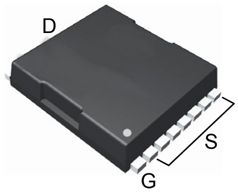
100V N-ChannelEnhancement Mode MOSFET

Features

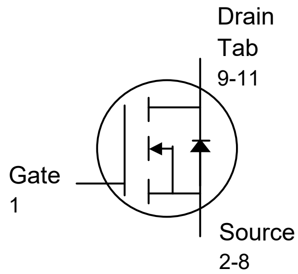
- Advanced Super Trench technology
- Low Gate Charge.
- Low On-Resistance
- Low Reverse transfer capacitances
- Fast Switching
- Reliable and Rugged
- Pb-free plating; RoHS compliant
- 100% avalanche energy Test



TOLL View

Applications

- Synchronous Rectification.
- Variable frequency pump controller.
- Brushless motor driver.
- Electric Motorcycle Driver.
- Uninterruptible Power Supply.
- Battery Management.



Schematic Diagram

Product Summary

Parameter	Value	Unit
V_{DS}	100	V
I_D @ V_{GS}= 10V	353	A
$R_{DS(ON)}$(typ.) @ V_{GS}=10V	1.3	mΩ

Order information

Product Name	Package	Media	Q'ty (pcs)
XPXGL300N10SHLL	TOLLA	Reel&Tape	2000

Absolute maximum ratings (at T_A = 25°C ,unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Drain Current -Continuous ① ④	T_C= 25°C	353	A
		T_C= 100°C	250	A
I_{DM}	Drain Current -Pulsed ②③	T_C= 25°C	1401	A
P_D	Maximum Power Dissipation	T_C= 25°C	375	W
		T_C= 100°C	188	W
I_S	Diode Continuous Forward Current	T_C= 25°C	278	A
E_{AS}	Avalanche Energy, Single pulse ⑤	L=0.5mH	1660	mJ
T_{stg}	Storage Temperature		-55 to 175	°C
Tj	Maximum Junction Temperature		175	°C

Thermal characteristics

Symbol	Parameter		Value	Unit
R_{thJ-C}	Junction to Case	Steady State	0.40	°C/W
R_{thJ-A}	Junction to Ambient ④	Steady State	36.0	°C/W

Note :

①,Calculated continuous current based on maximum allowable junction temperature.

②,Pulse width limited by maximum junction temperature.

③,UIS tested and pulse width limited by maximum junction temperature 150℃ (initial temperature Tj=25℃).

④,Surface Mounted on 1in^2 pad area.

⑤, EAS Condition :Tj=25℃,VD=50V VG=10V,L=0.5mH,Rg=25Ω.

Electrical Characteristics (T_c=25℃unless otherwise noted)

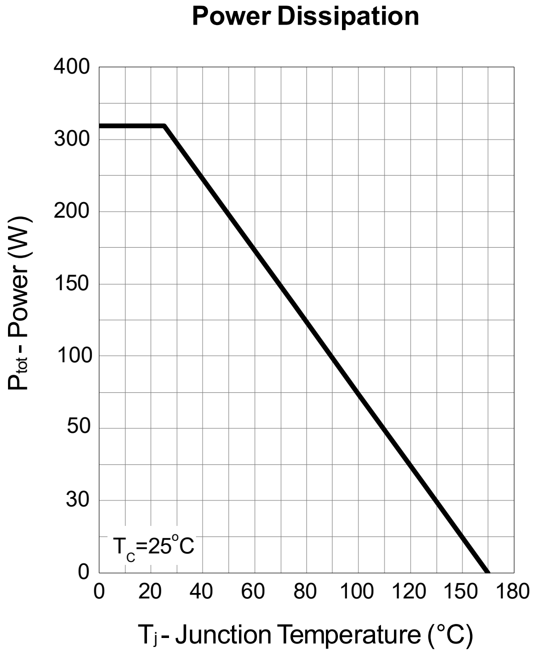
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=80V,V_{GS}=0V,Tj=85℃	-	-	30	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	2.0	3.0	4.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance (1)	V_{GS}=10V, I_D=40A	-	1.3	1.7	mΩ
Dynamic Characteristics (2)						
R_g	Gate Resistance	V_{GS}=V_{DS}=0V. f=1MHz	-	0.5	-	Ω
C_{iss}	Input Capacitance	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	12500	16000	PF
C_{oss}	Output Capacitance		-	4644	-	PF
C_{rss}	Reverse Transfer Capacitance		-	2672	-	PF
Switching Characteristics (2)						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=50V, R_L=30Ω. I_D=1A, V_{GS}=10V, R_G=6Ω.	-	85	-	nS
t_r	Turn-on Rise Time		-	45	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	280	-	nS
t_f	Turn-Off Fall Time		-	120	-	nS
Gate Charge Characteristics (2)						
Q_g	Total Gate Charge	V_{DS}=50V, I_D=40A, V_{GS}=10V.	-	210	-	nC
Q_{gs}	Gate-Source Charge		-	65	-	nC
Q_{gd}	Gate-Drain Charge		-	51	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage (1)	V_{GS}=0V,I_S=40A	-	0.7	1.3	V
trr	Reverse Recovery Time	T_J=25°C, I_S=40A, di/dt =100A/μs	-	180	-	nS
Qrr	Reverse Recovery Charge		-	480	-	nC

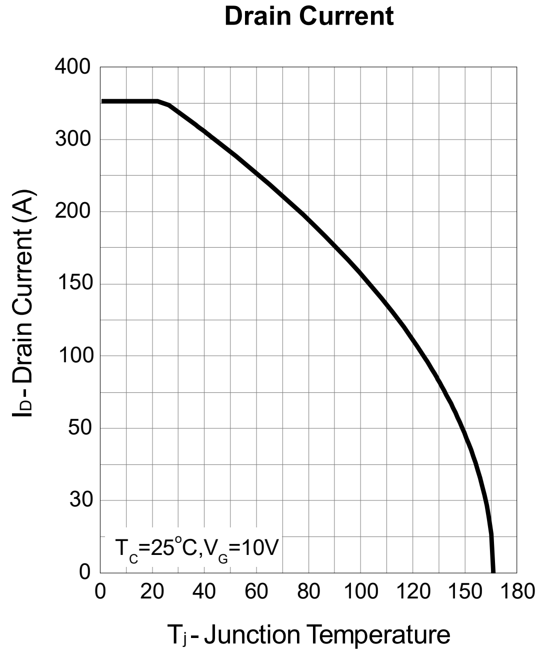
Note:

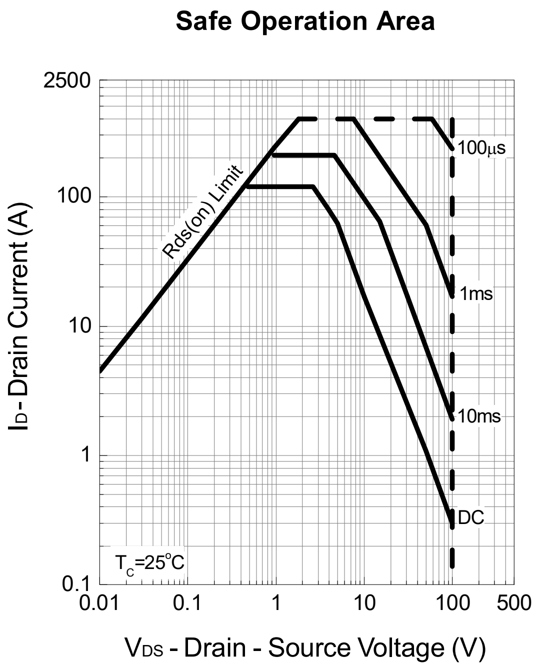
(1)：Pulse test ; pulse width≤300μs, duty cycle≤2%.

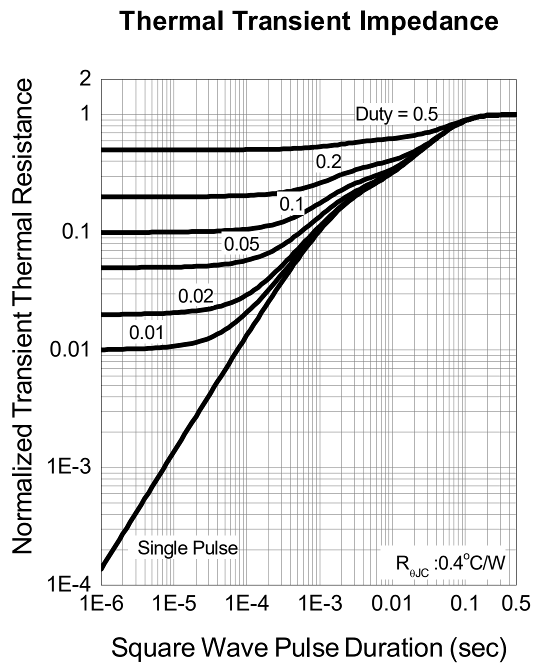
(2)：Guaranteed by design, not subject to production testing.

Typical Operating Characteristics



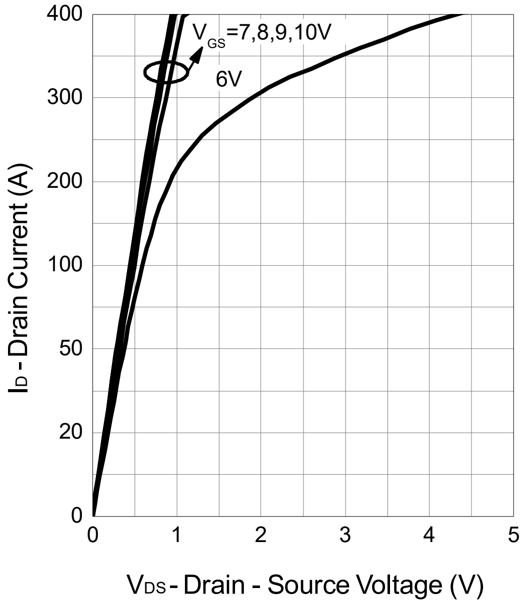




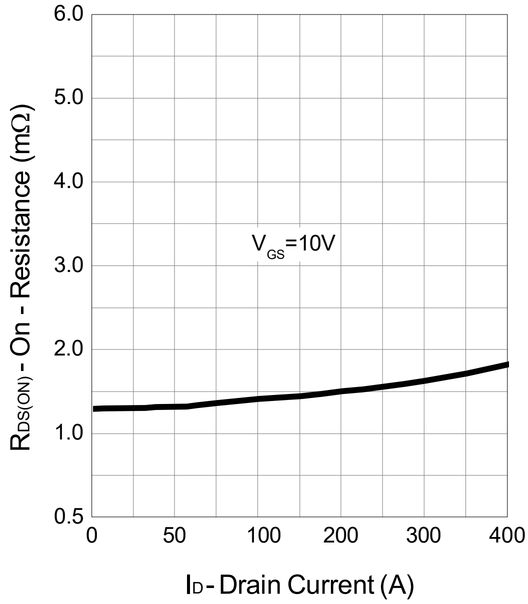


Typical Operating Characteristics

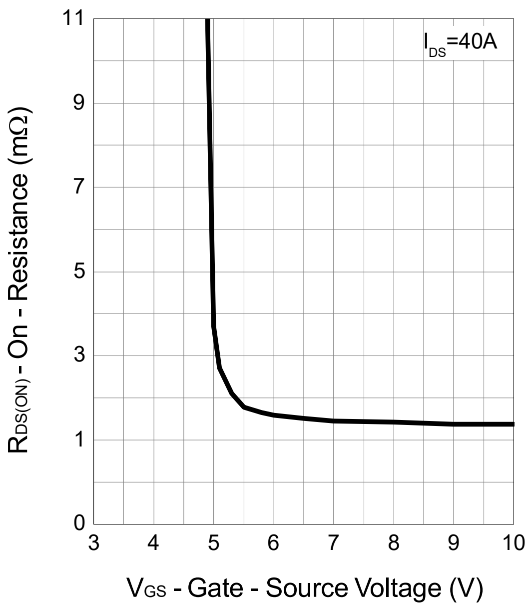
Output Characteristics



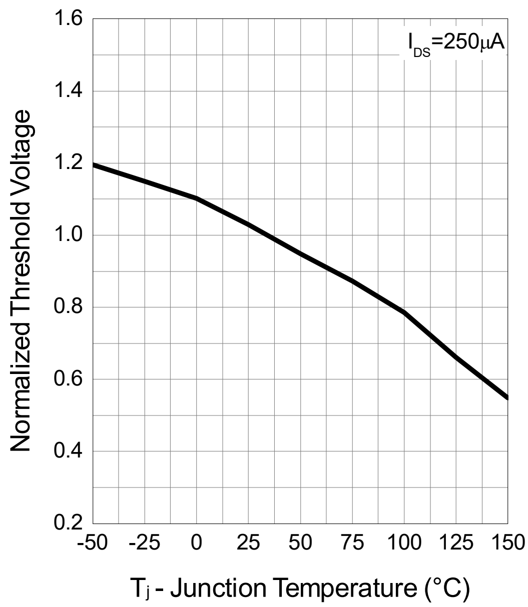
Drain-Source On Resistance



Gate-Source On Resistance

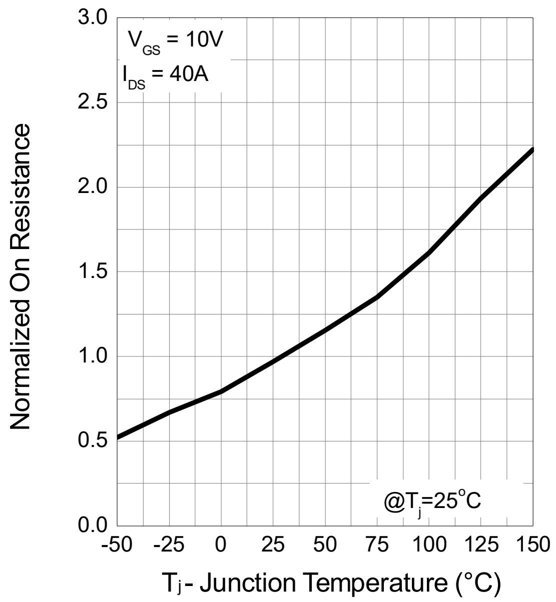


Gate Threshold Voltage

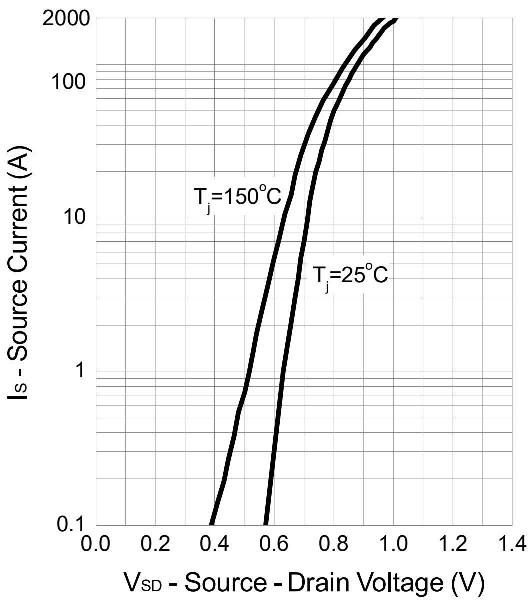


Typical Operating Characteristics

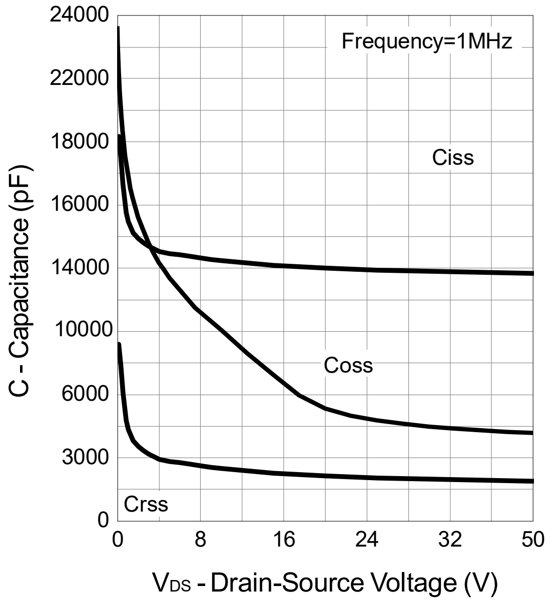
Drain-Source On Resistance



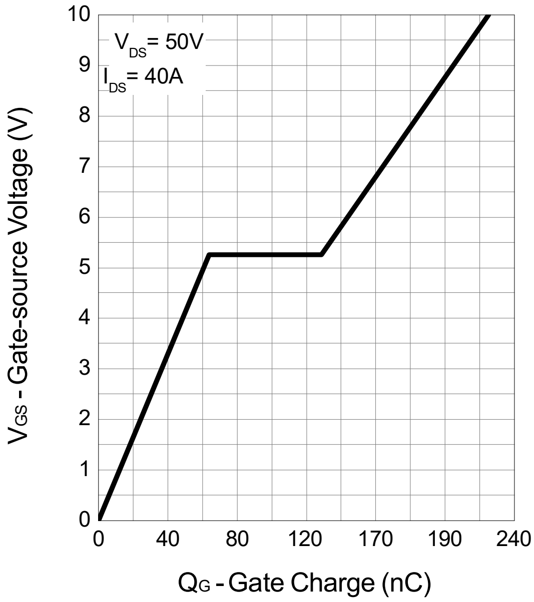
Source-Drain Diode Forward

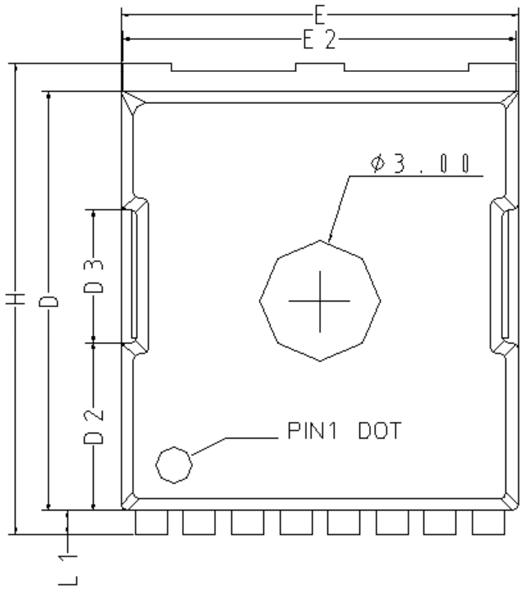


Capacitance

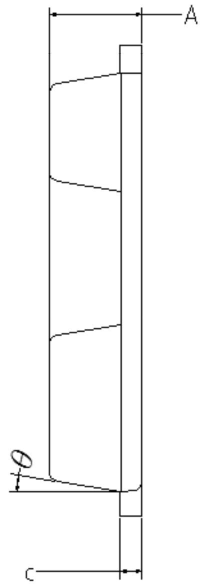


Gate Charge

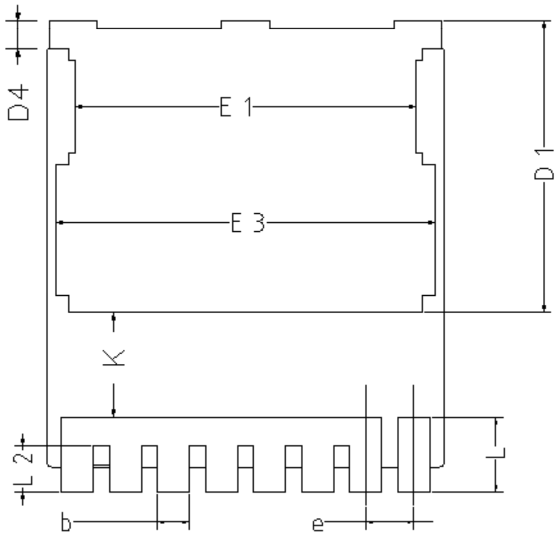




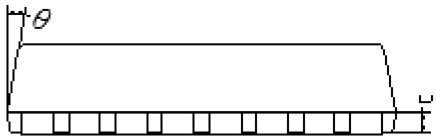
Top View



Side View



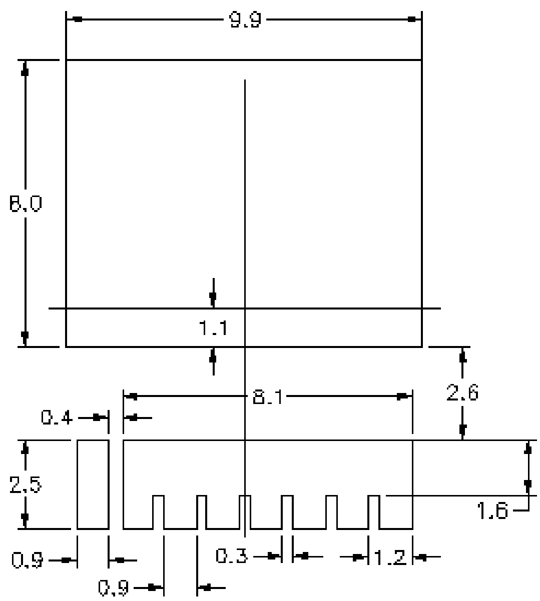
Bottom View



Side View

SYMBOLS	TO-LL			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
c	0.40	0.60	0.016	0.024
D	10.23	10.63	0.403	0.419
D1	7.05	7.45	0.278	0.293
D2	3.98	4.38	0.157	0.172
D3	3.10	3.50	0.122	0.138
D4	0.50	0.90	0.020	0.035
E	9.70	10.10	0.382	0.398
E1	8.30	8.70	0.327	0.343
E2	9.60	10.00	0.378	0.394
E3	9.26	9.66	0.365	0.380
H	11.53	11.93	0.454	0.470
e	1.2 BSC		0.0472 BSC	
K	2.43	2.83	0.096	0.111
L	1.65	2.05	0.065	0.081
L1	0.40	0.80	0.016	0.031
L2	0.95	1.35	0.037	0.053
θ	6°	10°	6°	10°

RECOMMENDED LAND PATTERN



UNIT: mm

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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