60V N-Channel Enhancement Mode MOSFET

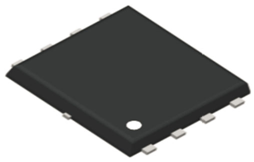
Description

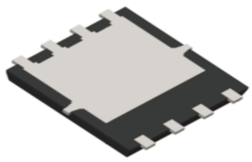
The XPX80N06RD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

V_{DS} =60V, I_D =80A

$R_{DS(ON)}$=7.3mΩ (typ) @ V_{GS}=10V

$R_{DS(ON)}$=10mΩ (typ) @ V_{GS}=4.5V

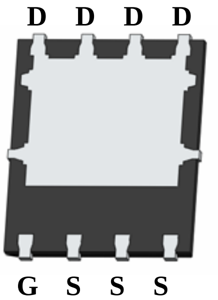


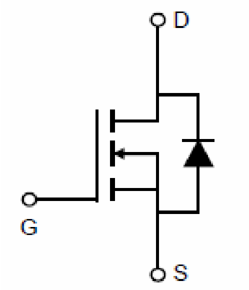


General Features

V_{DS} = 60V I_D =80A

$R_{DS(ON)}$ < 7.3mΩ @ V_{GS}=10V





Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX80N06RD	PDFN5*6-8L	XPX80N06 XXX YYYY	5000

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Value	Unit
VDS	Drain source voltage	60	V
VGS	Gate source voltage	±20	V
ID	Continuous drain current[1)]	80	A
ID, pulse	Pulsed drain current[2)]	138	A
P_D	Power dissipation[3)]	60	W
EAS	Single pulsed avalanche energy[4)]	30	mJ
Tstg，Tj	Operation and storage temperature	-55 to 150	℃
RθJC	Thermal resistance, junction-case	2.1	°C/W
RθJA	Thermal resistance, junction-ambient[5)]	62	°C/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BVDSS	Drain-source breakdown voltage	V_{GS}=0 V, I_D=250 μA	60	68		V
VGS(th)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 μA	1.2	1.5	2.5	V
RDS(ON)	Drain-source on-state resistance	V_{GS}=10 V, I_D=20 A		7.3	10	mΩ
RDS(ON)	Drain-source on-state resistance	V_{GS}=4.5 V, I_D=10 A		10	13	mΩ
IGSS	Gate-source leakage current	V_{GS}=±20 V			±100	nA
IDSS	Drain-source leakage current	V_{DS}=60 V, V_{GS}=0 V			1	μA
Ciss	Input capacitance	V_{GS}=0 V, V_{DS}=50 V, *f*=100 kHz		1193.1		pF
Coss	Output capacitance			199.5		pF
Crss	Reverse transfer capacitance			4.1		pF
td(on)	Turn-on delay time	V_{GS}=10 V, V_{DS}=50 V, R_G=2 Ω, I_D=10 A		17.9		ns
t_r	Rise time			4.0		ns
td(off)	Turn-off delay time			34.9		ns
t_f	Fall time			5.5		ns
Q_g	Total gate charge	I_D=10 A, V_{DS}=50 V, V_{GS}=10 V		18.4		nC
Q_{gs}	Gate-source charge			3.3		nC
Qgd	Gate-drain charge			3.1		nC
Vplateau	Gate plateau voltage			2.8		V
I_S	Diode forward current	VGS<Vth			60	A
ISP	Pulsed source current				180	
VSD	Diode forward voltage	I_S=20 A, V_{GS}=0 V			1.3	V
trr	Reverse recovery time	I_S=10 A, di/dt=100 A/μs		41.8		ns
Q_{rr}	Reverse recovery charge			36.1		nC
Irrm	Peak reverse recovery current			1.4		A

Note

1、Calculated continuous current based on maximum allowable junction temperature.

2、Repetitive rating; pulse width limited by max. junction temperature.

3、Pd is based on max. junction temperature, using junction-case thermal resistance.

4、V_{DD}=50 V, R_G=50 Ω, L=0.3 mH, starting T_j=25 ℃.

5、The value of $R_{θJA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 ℃.

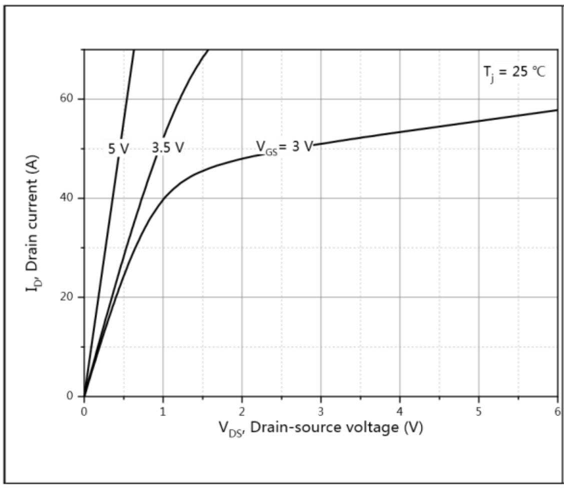


Figure 1, Typ. output characteristics

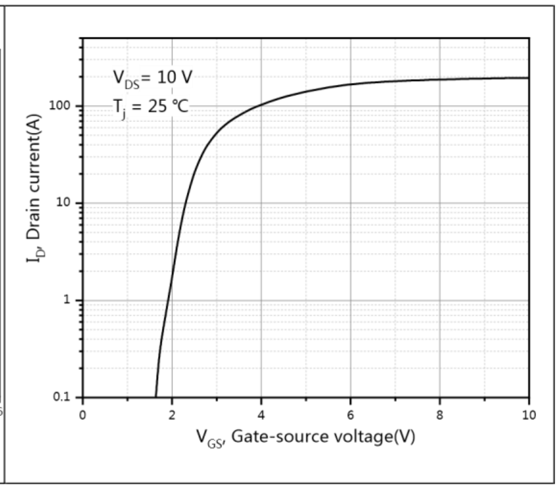


Figure 2, Typ. transfer characteristics

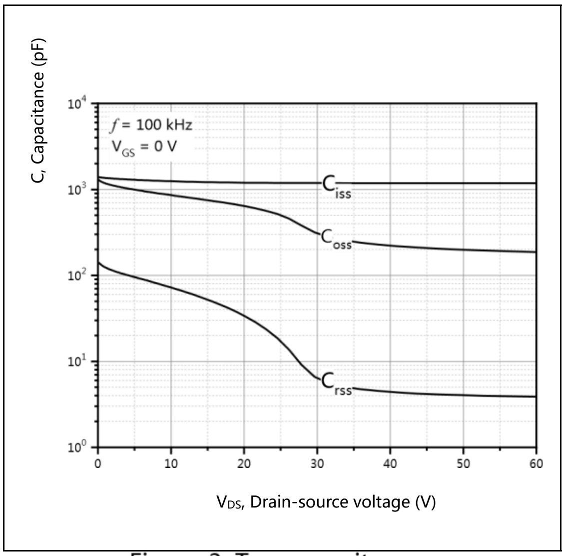


Figure 3, Typ. capacitances

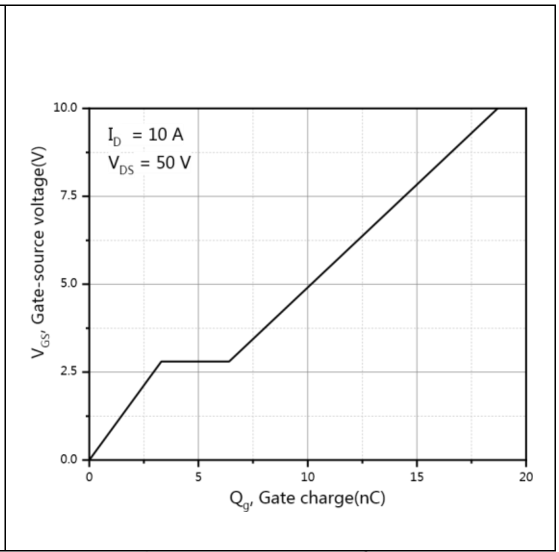


Figure 4, Typ. gate charge

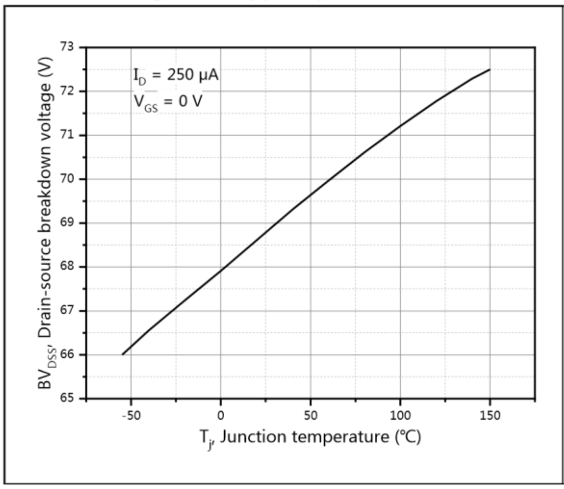


Figure 5, Drain-source breakdown voltage

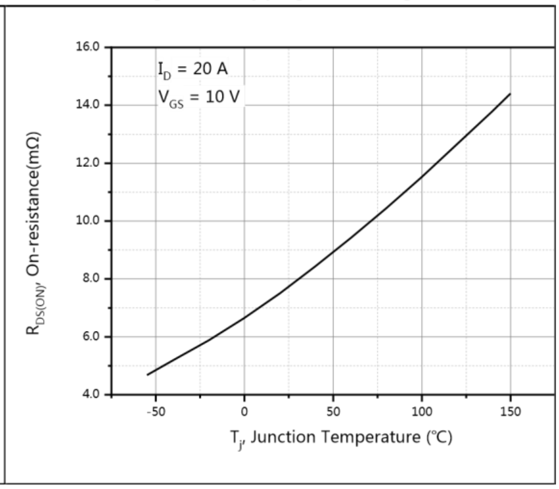
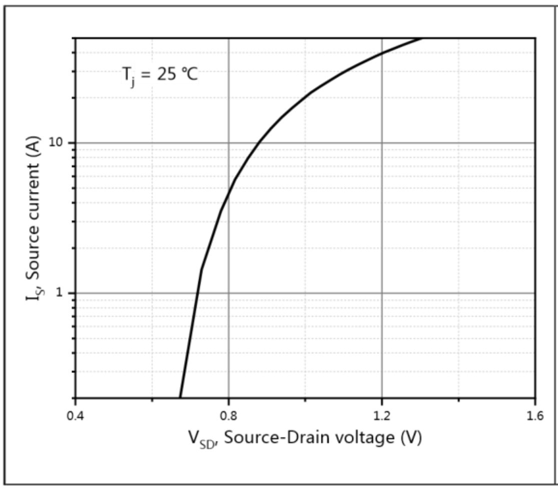


Figure 6, Drain-source on-state resistance



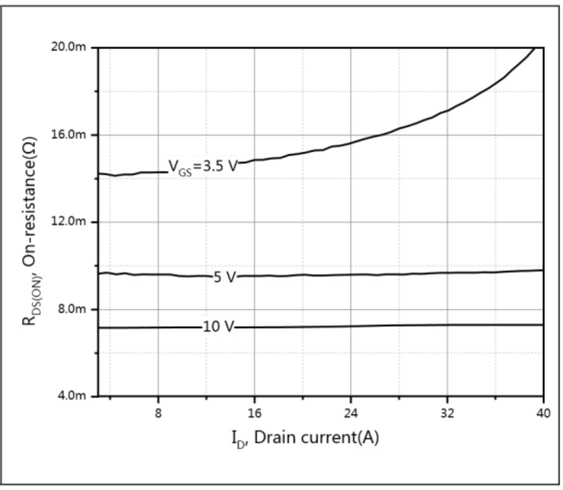


Figure 7, Forward characteristic of body diode

Figure 8, Drain-source on-state resistance

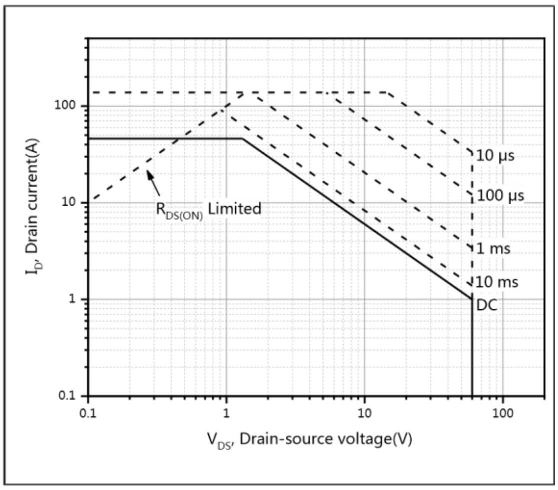
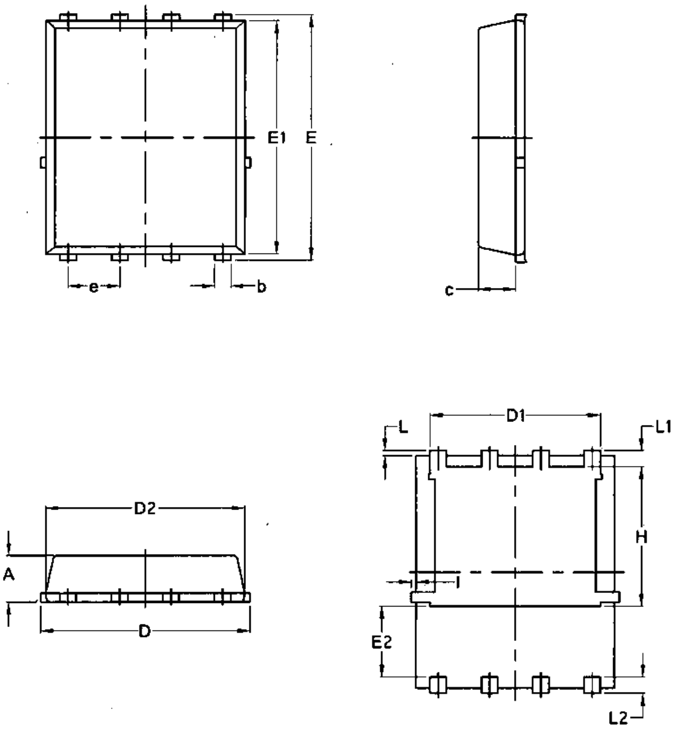


Figure 9, Safe operation area T_C=25 ℃

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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