60V N-ChannelEnhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX60N013LL uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

V_{DS} =60V,I_D =280A

$R_{DS(ON)}$=1.3mΩ (typ) @ V_{GS}=10V

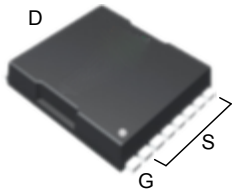
$R_{DS(ON)}$=1.6mΩ (typ) @ V_{GS}=4.5V

General Features

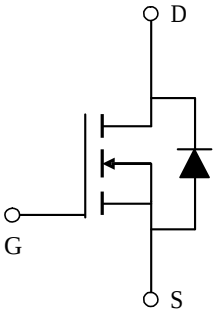
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching



TO-LL



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX60N013LL	XPX60N013LL	TO-LL	-	-	2000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	280	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	226	A
Pulsed Drain Current	I_{DM}	1180	A
Maximum Power Dissipation	P_D	296	W
Derating factor		1.99	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	2040	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.58	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

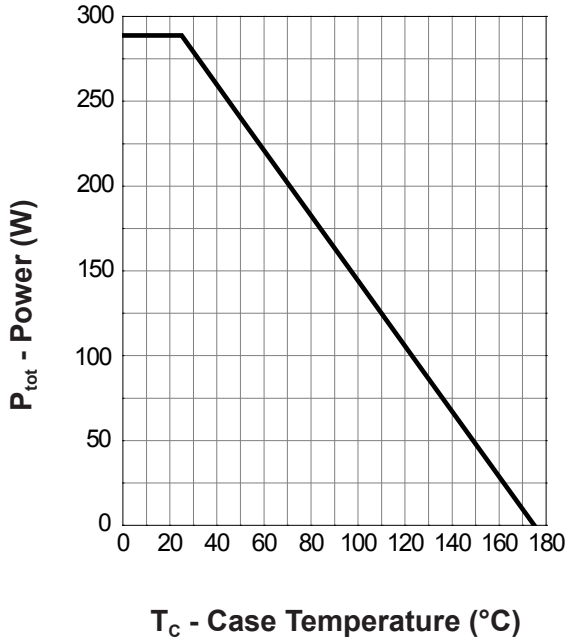
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=60A	-	1.3	1.6	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=60A	-	70	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	8689	-	PF
Output Capacitance	C_{oss}		-	1246	-	PF
Reverse Transfer Capacitance	C_{rss}		-	694	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω, R_G=2.5Ω,V_{GS}=10V	-	35	-	nS
Turn-on Rise Time	t_r		-	25	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g	I_D=30A,V_{DD}=30V,V_{GS}=10V	-	197	-	nC
Gate-Source Charge	Q_{gs}		-	46	-	nC
Gate-Drain Charge	Q_{gd}		-	57	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=60A	-	0.8	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	280	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 60A di/dt = 100A/μs(Note3)	-	33		nS
Reverse Recovery Charge	Qrr		-	84		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

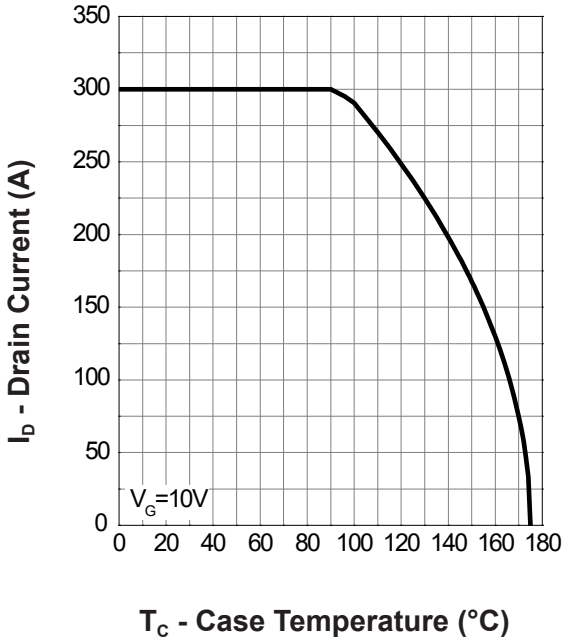
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=30V,V_G=10V,L=1mH,Rg=25Ω

Typical Operating Characteristics

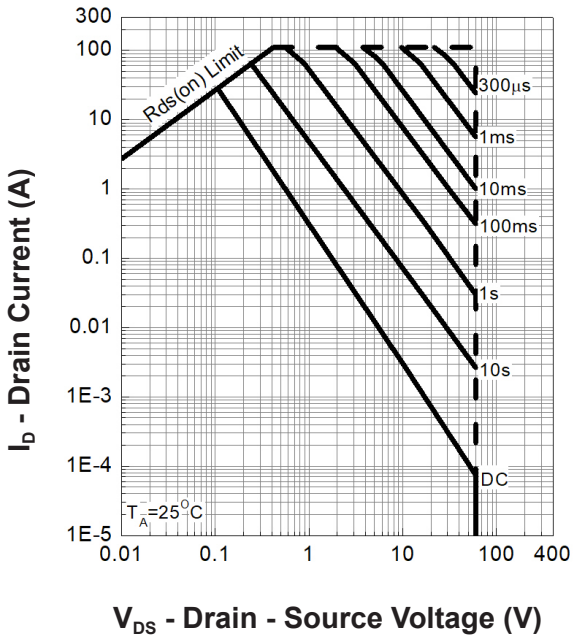
Power Dissipation



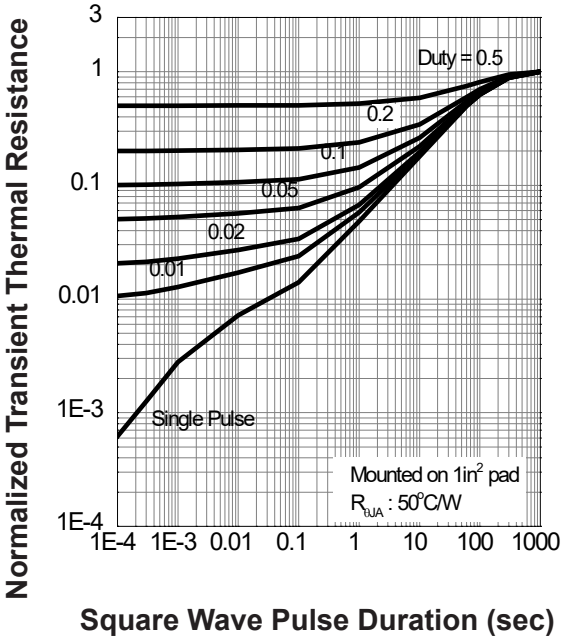
Drain Current



Safe Operation Area

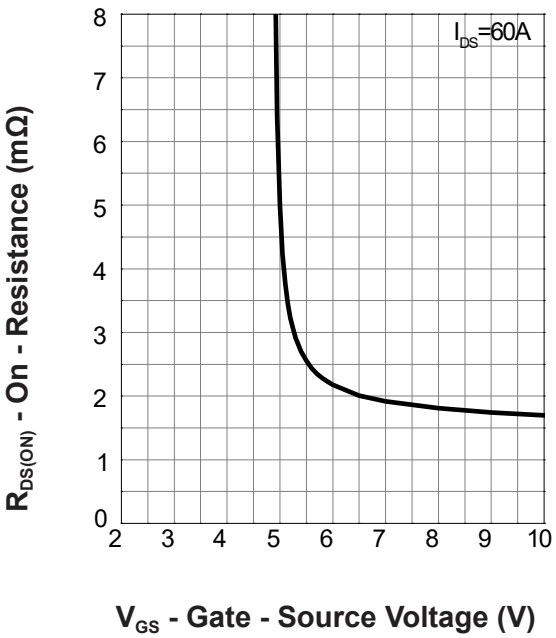


Thermal Transient Impedance

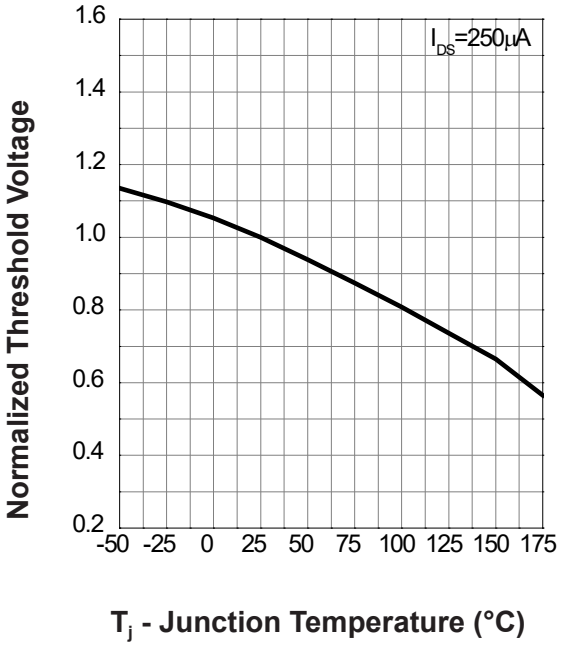


Typical Operating Characteristics(Cont.)

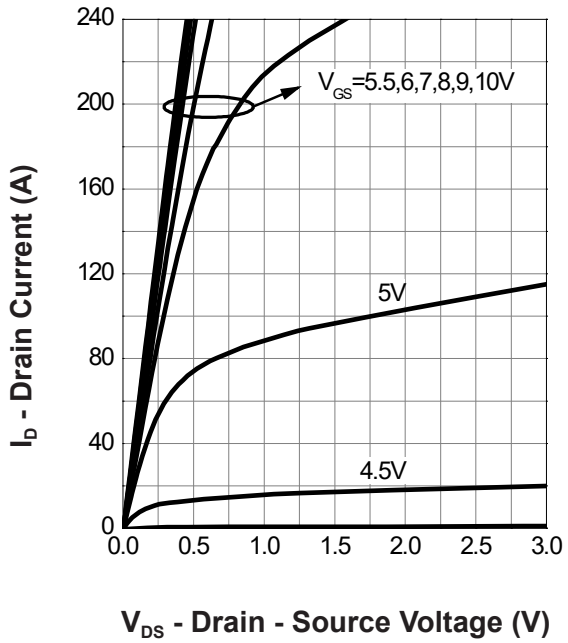
Gate-Source On Resistance



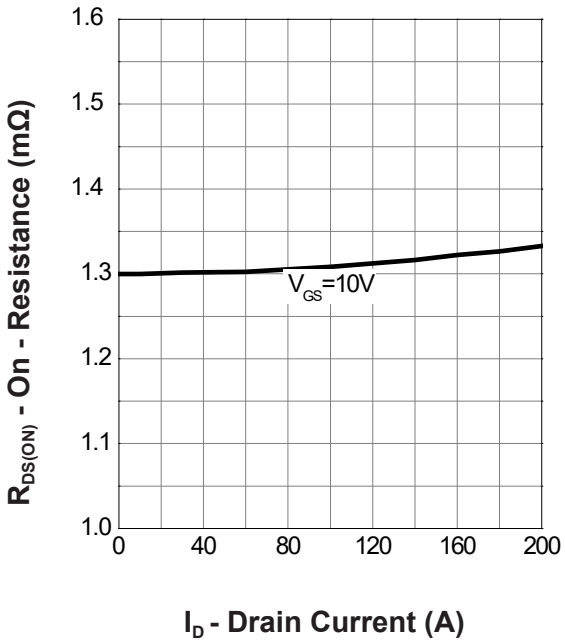
Gate Threshold Voltage



Output Characteristics

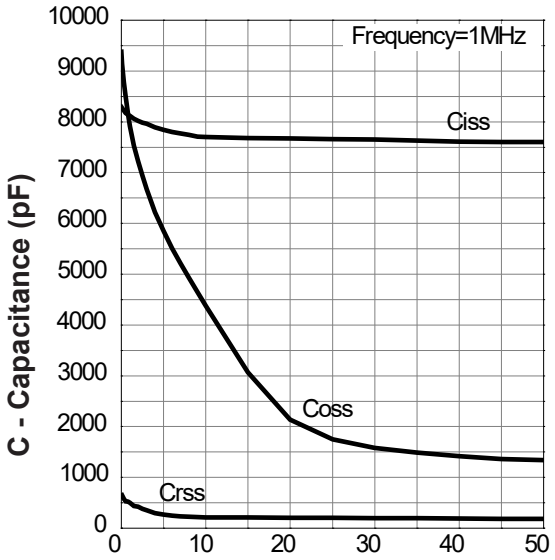


Drain-Source On Resistance

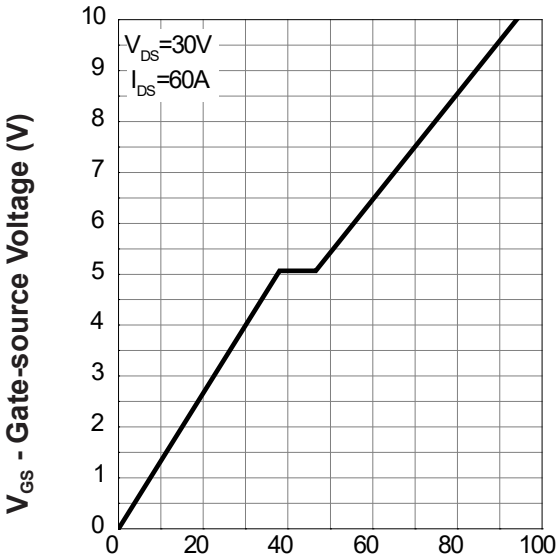


Typical Operating Characteristics(Cont.)

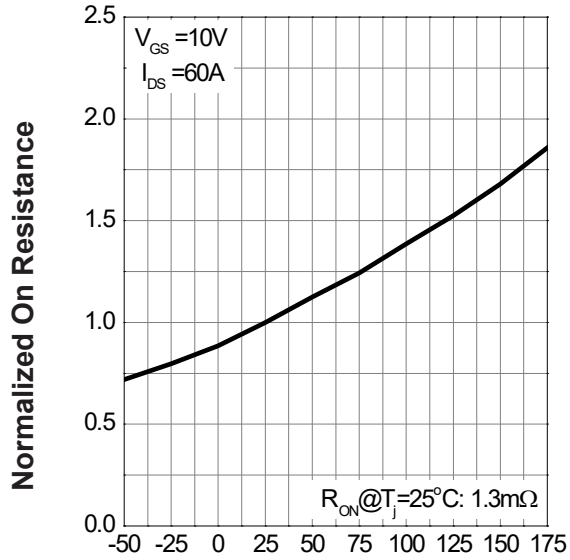
Capacitance



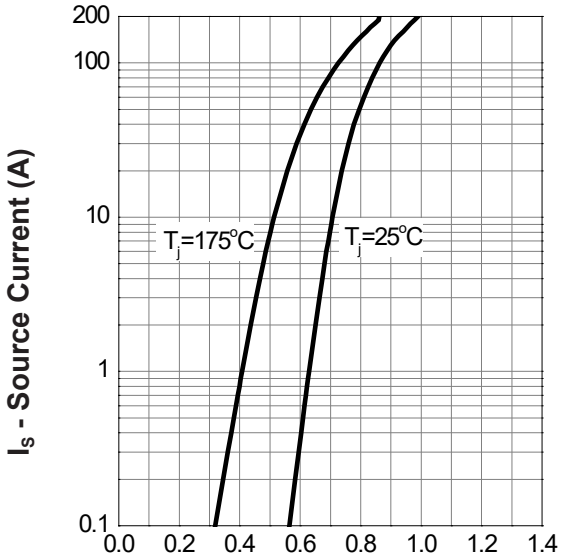
Gate Charge



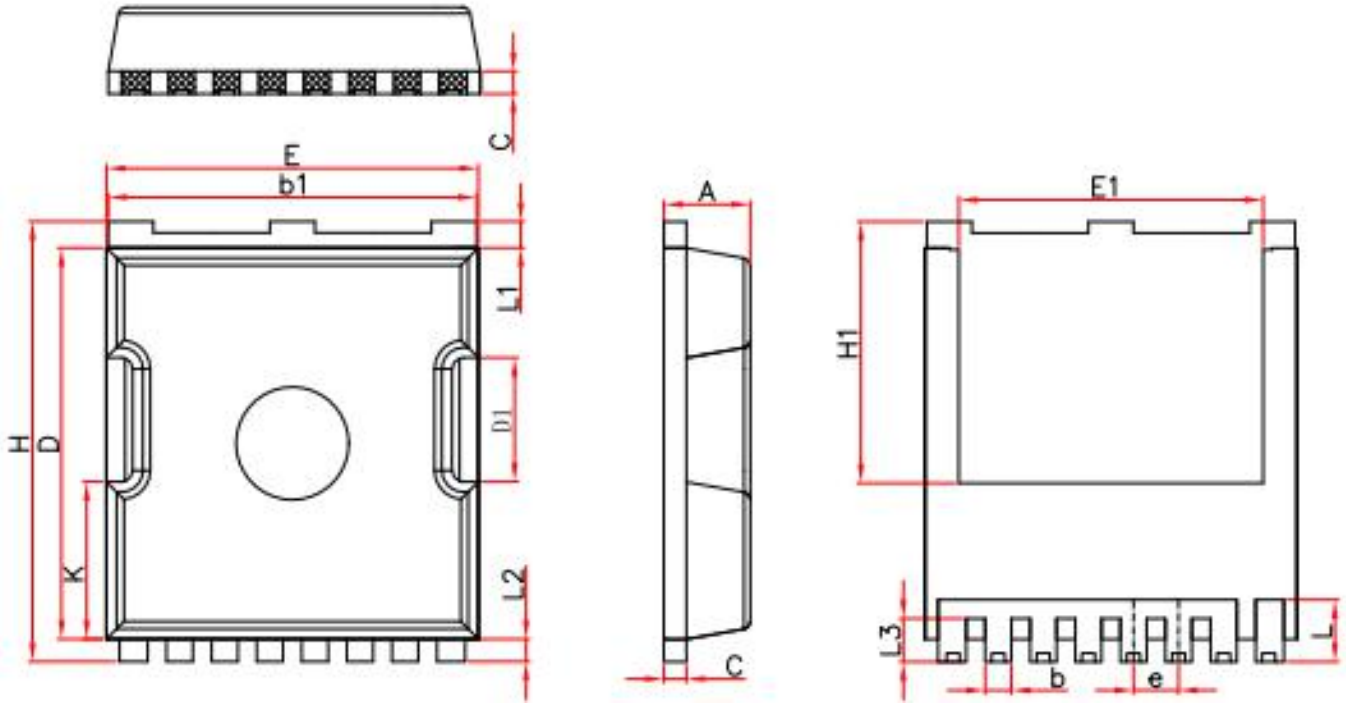
Drain-Source On Resistance



Source-Drain Diode Forward



TOLL Package Information



Symbol	Millimeters		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
b	0.65	0.75	0.85
b1	9.70	9.80	9.90
C	0.50	0.60	0.70
D	10.30	10.40	10.50
D1	3.15	3.3	3.45
E	9.70	9.90	10.10
E1	8.00	8.10	8.20
e	1.10	1.20	1.30
H	11.6	11.7	11.8
H1	6.85	6.95	7.05
K	4.08	4.18	4.28
L	1.60	1.65	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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