40V N-Channel Super Trench Power MOSFET

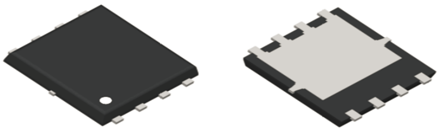
Description

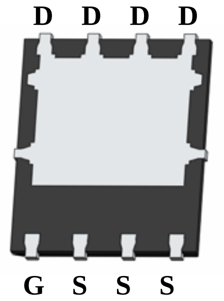
The XPX4N1U5RD uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

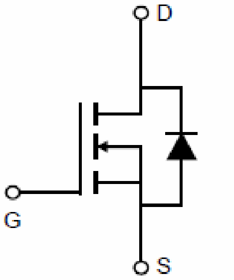
V_{DS} =40V,I_D =150A

$R_{DS(ON)}$=1.5mΩ (typ) @ V_{GS}=10V

$R_{DS(ON)}$=1.9mΩ (typ) @ V_{GS}=4.5V







General Features

- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX4N1U5RD	XPX4N1U5RD	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous **(Silicon Limited)**	I_D	150	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	119	A
Pulsed Drain Current **(Package Limited)**	I_{DM}	420	A
Maximum Power Dissipation	P_D	88	W
Derating factor		0.9	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	600	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.55	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.6	2.3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=80A	-	1.5	1.8	mΩ
		V_{GS}=4.5V, I_D=75A	-	1.9	2.3	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=75A		80	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{Iss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	3698	6888	PF
Output Capacitance	C_{oss}		-	1586	1695	PF
Reverse Transfer Capacitance	C_{rss}		-	100	148	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=75A V_{GS}=10V,R_G=1.6Ω	-	12.5	-	nS
Turn-on Rise Time	t_r		-	7.0	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t_f		-	8.5	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=75A, V_{GS}=10V	-	95	115	nC
Gate-Source Charge	Q_{gs}		-	15		nC
Gate-Drain Charge	Q_{gd}		-	11		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=75A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	150	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs(Note3)	-		31	nS
Reverse Recovery Charge	Qrr		-		110	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω

Typical Electrical and Thermal Characteristics

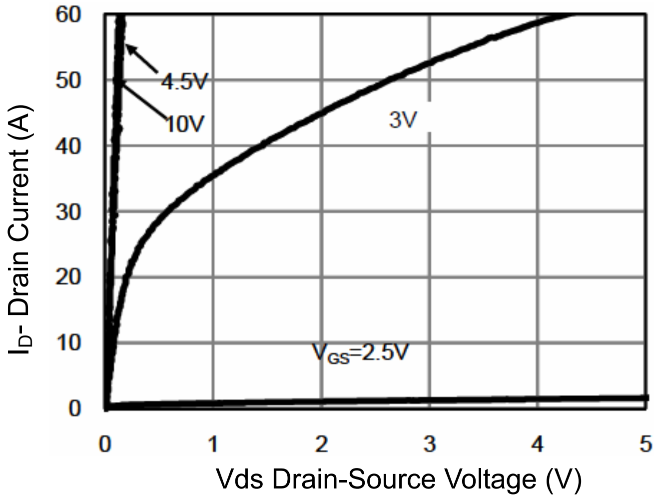


Figure 1 Output Characteristics

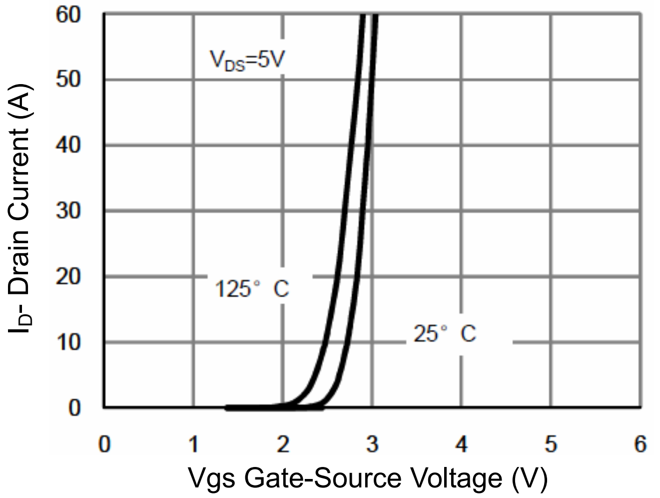


Figure 2 Transfer Characteristics

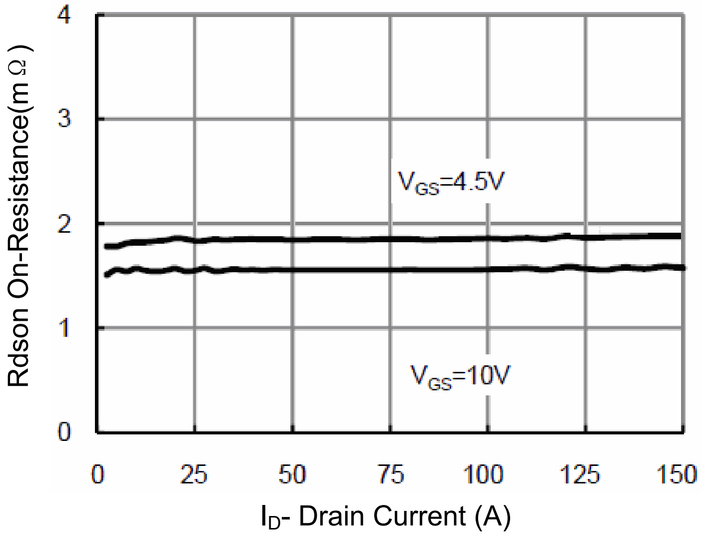


Figure 3 Rdson- Drain Current

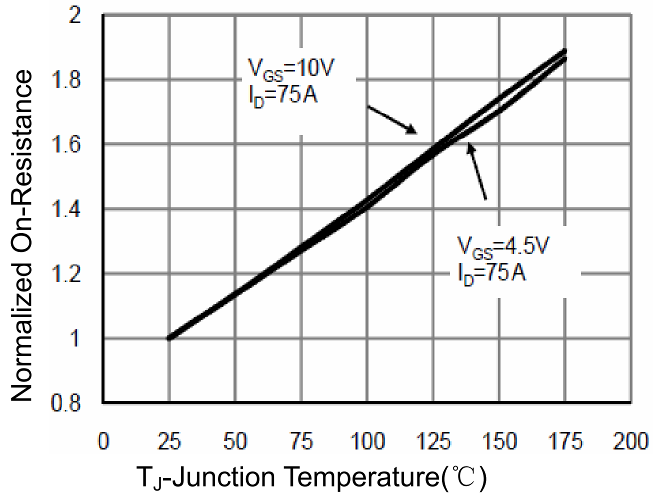


Figure 4 Rdson-JunctionTemperature

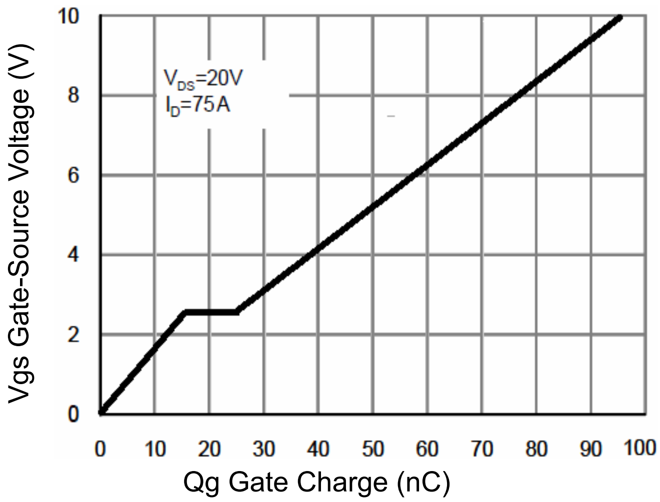


Figure 5 Gate Charge

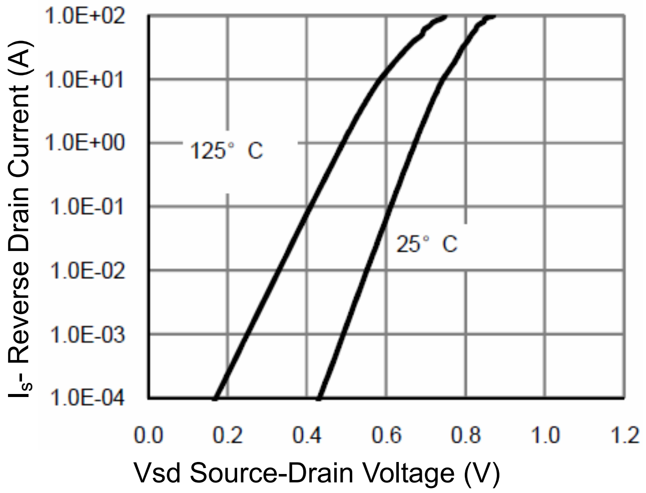


Figure 6 Source- Drain Diode Forward

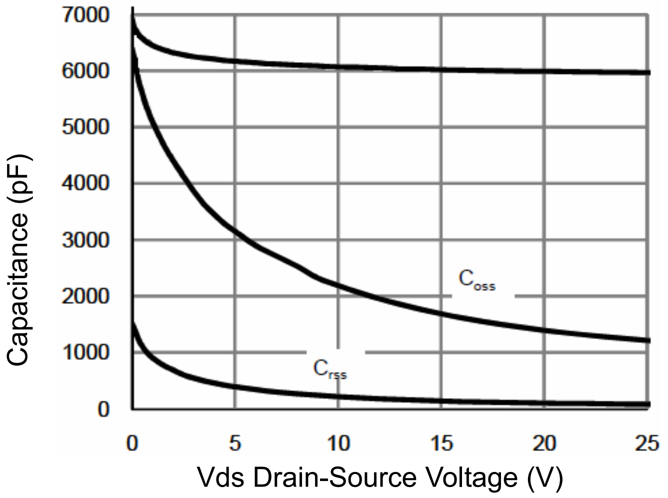


Figure 7 Capacitance vs Vds

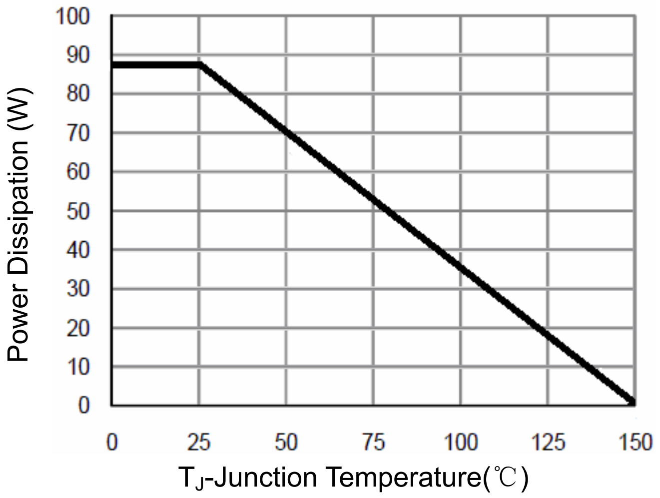


Figure 9 Power De-rating

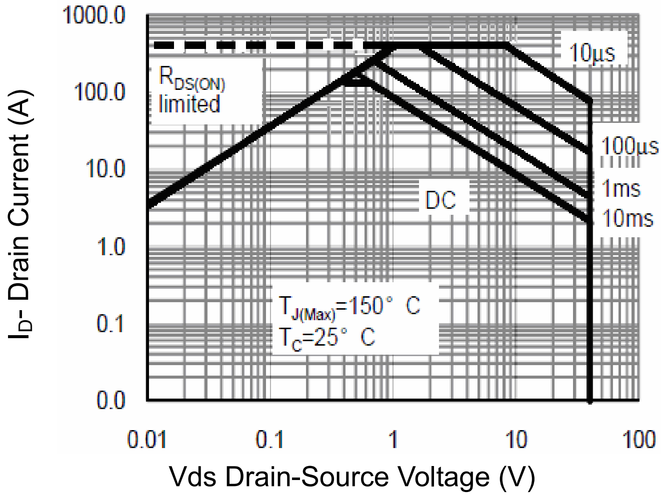


Figure 8 Safe Operation Area

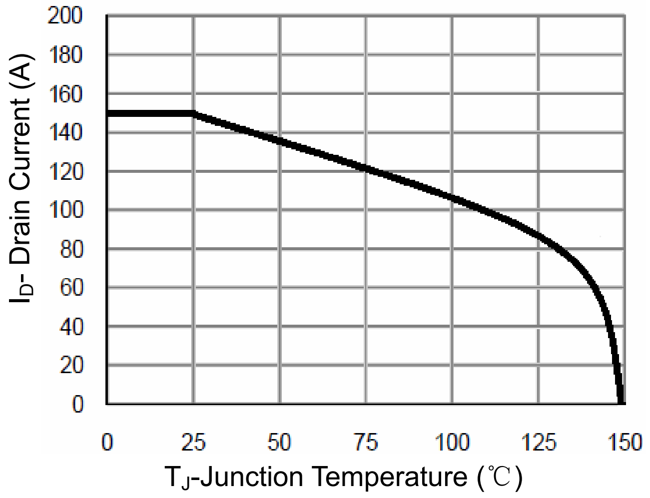


Figure 10 Current De-rating

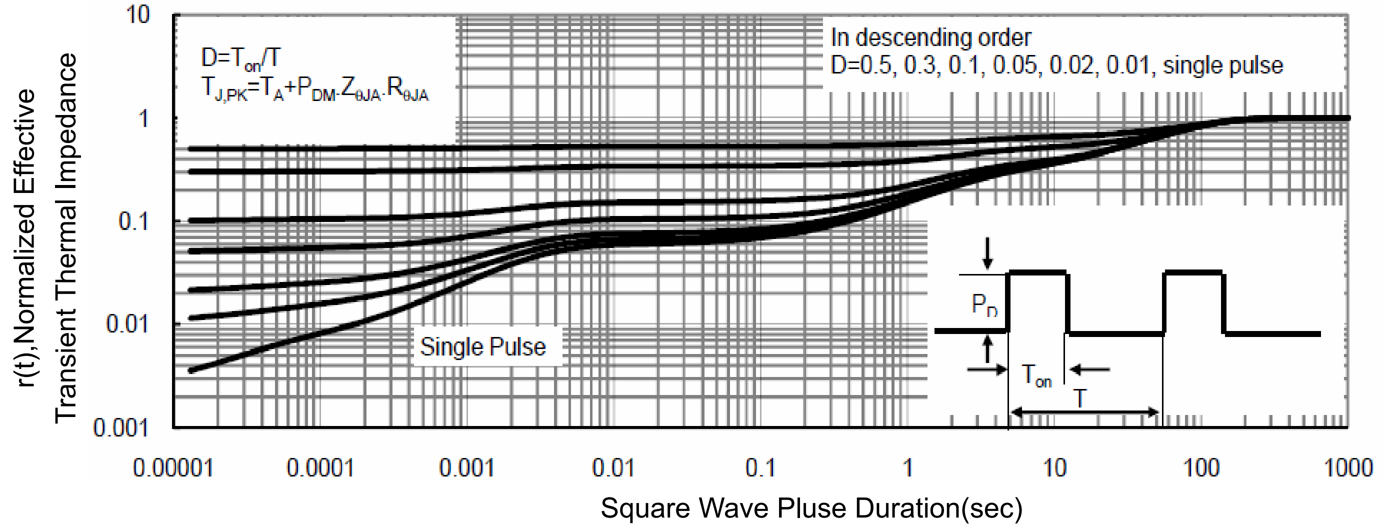
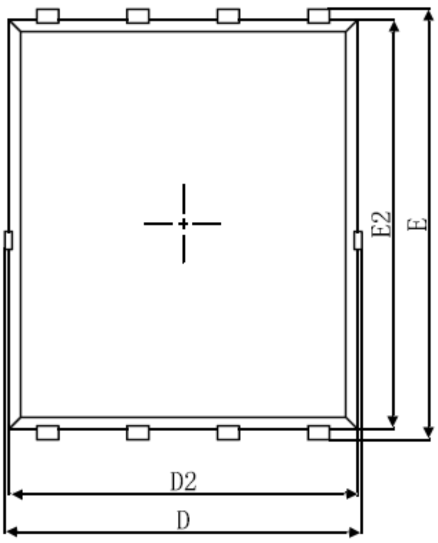
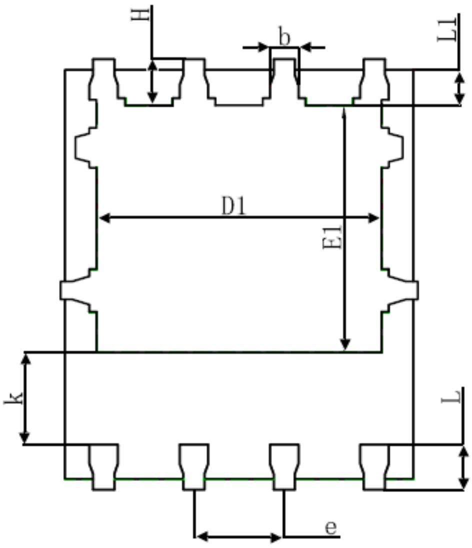


Figure 11 Normalized Maximum Transient Thermal Impedance

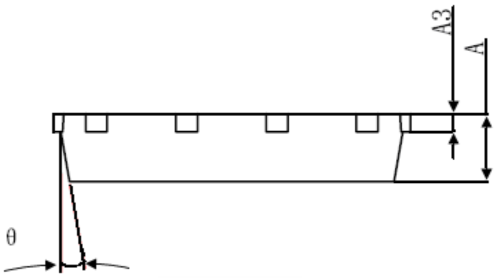
DFN5X6-8L Package Information



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.