100V N-ChannelEnhancement Mode MOSFET

Description

The XPX450N10LL uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

V_{DS} =40V,I_D =450A

$R_{DS(ON)}$=0.9mΩ (typ) @ V_{GS}=10V

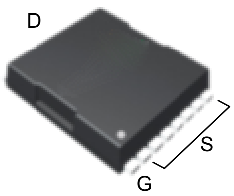
$R_{DS(ON)}$=1.2mΩ (typ) @ V_{GS}=6V

General Features

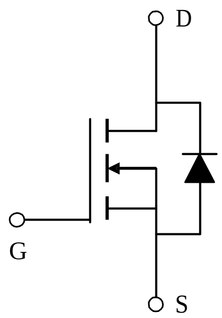
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching



TO-LL



Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C=25℃	-	100	V
V_{GS}	Gate-Source Voltage	T_C=25℃	-	±20	V
I_D *	Drain Current (DC)	T_C=25℃, V_{GS}=10 V	-	450	A
		T_C=100℃, V_{GS}=10 V	-	290	A
I_{DM} *,**	Drain Current (Pulsed)	T_C=25℃, V_{GS}=10 V	-	1840	A
P_D	Power Dissipation	T_C=25℃	-	513	W
I_S	Continuous-Source Current	T_C=25℃	-	450	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=75 V, L=0.3 mH	-	1750	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	℃
$R_{θJA}$ **	Thermal Resistance-Junction to Ambient		-	40	℃/W
$R_{θJC}$ **	Thermal Resistance-Junction to Case		-	0.35	℃/W

Package Marking and Ordering Information

Device	Pack	Marking	Qty(PCS)
XPX450N10LL	TOLL	XPX450N10LL XXXX YYYY	

Electrical Characteristics (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V, I_{DS}=250 μA	100	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250 μA	2.2	-	3.5	V
I_{DSS}	Drain Leakage Current	V_{DS}=100 V, V_{GS}=0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS}=0 V, V_{GS}=±20 V	-	-	±100	nA
$R_{DS(ON)}$ [a]	On-State Resistance	V_{GS}=10 V, I_{DS}=50 A	-	0.9	1.2	mΩ
		V_{GS}=6 V, I_{DS}=30 A	-	1.2	1.65	mΩ
g_{fs}	Forward Transconductance	V_{DS}=5 V, I_{DS}=30 A	-	49	-	S
R_g	Gate Resistance		-	1	2	Ω
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	V_{GS}=0 V, I_{SD}=30 A	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	V_{DS}=50 V, V_{GS}=0 V, I_{DS}=30 A, di/dt=100 A/μs	-	113	-	ns
Q_{rr}	Reverse Recovery Charge		-	400	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS}=50 V, V_{GS}=0 V, f=1 MHz	-	15622	-	pF
C_{oss}	Output Capacitance		-	2152	-	
C_{rss}	Reverse Transfer Capacitance		-	48	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50 V, V_{GEN}=10 V, R_G=6 Ω, I_{DS}=30 A	-	65	-	ns
t_r	Turn-on Rise Time		-	60	-	
$t_{d(off)}$	Turn-off Delay Time		-	223	-	
t_f	Turn-off Fall Time		-	104	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=50 V, V_{GS}=10 V, I_{DS}=30 A	-	275	-	nC
Q_{gs}	Gate-Source Charge		-	62	-	
Q_{gd}	Gate-Drain Charge		-	72	-	

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

ypical Characteristics

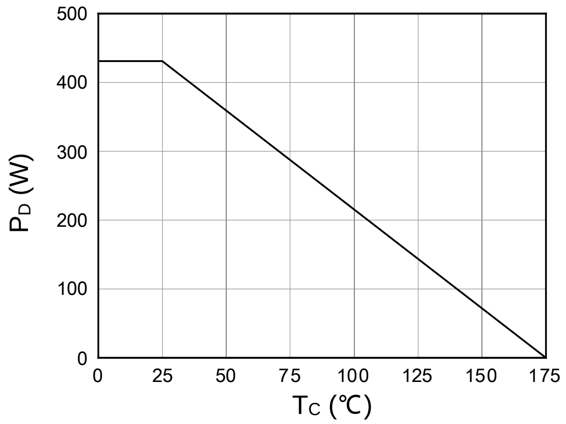


Figure 1. Power Capability

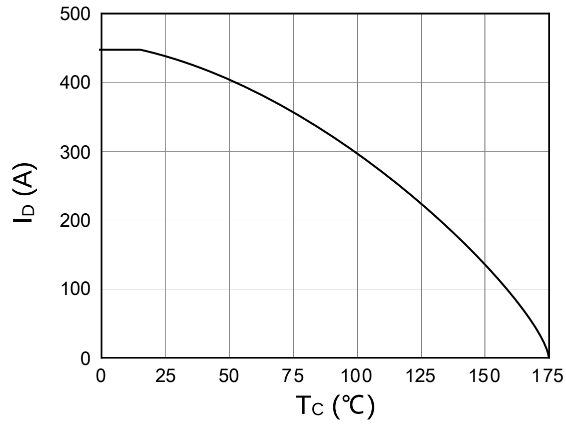


Figure 2. Current Capability

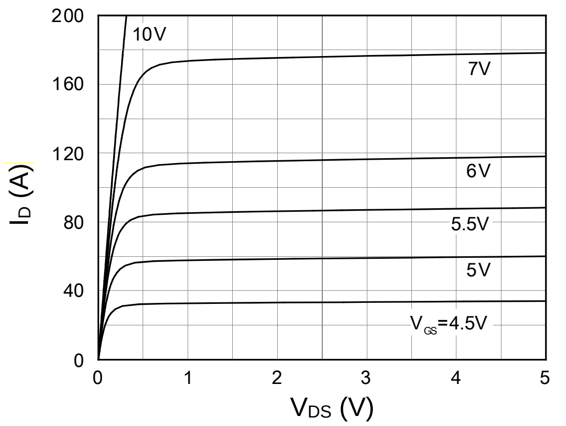


Figure 3. Output characteristics

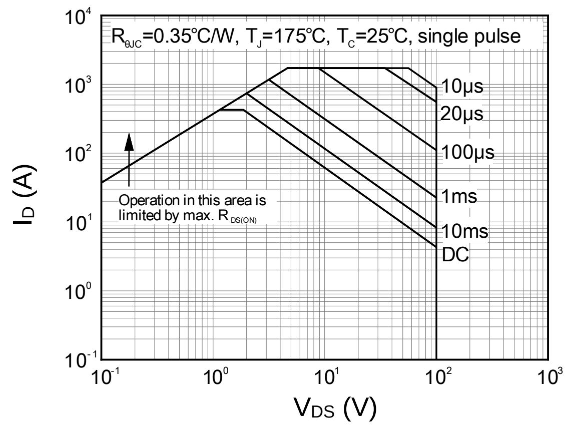


Figure 4. Safe operating area

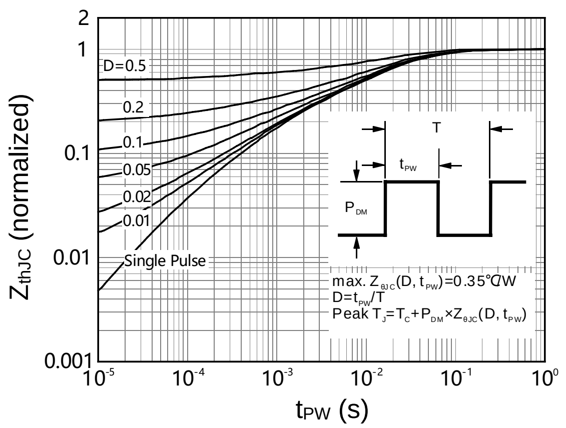


Figure 5. Normalized transient thermal impedance from junction to case

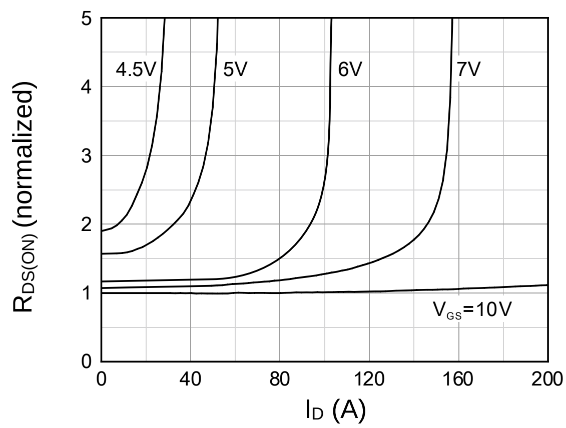


Figure 6. Normalized on-resistance vs drain current

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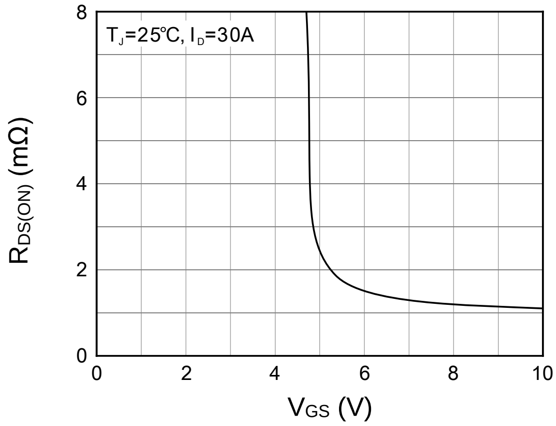


Figure 7. On-resistance vs gate-source voltage

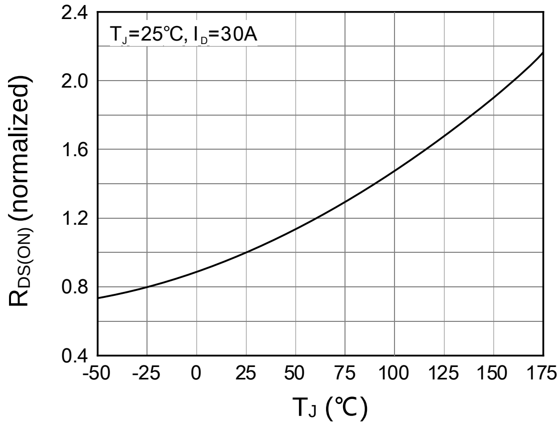


Figure 8. Normalized on-resistance vs junction temperature

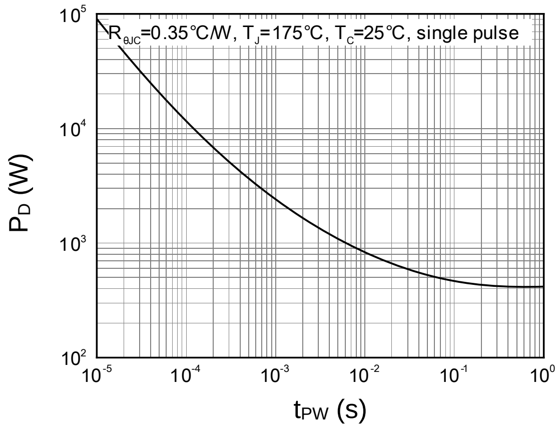


Figure 9. Single pulse maximum power dissipation

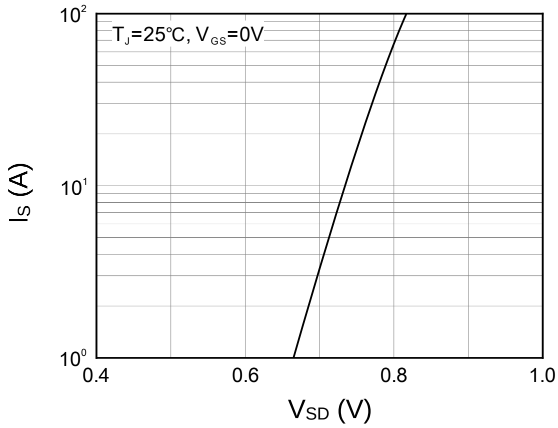


Figure 10. Forward characteristics of body diode

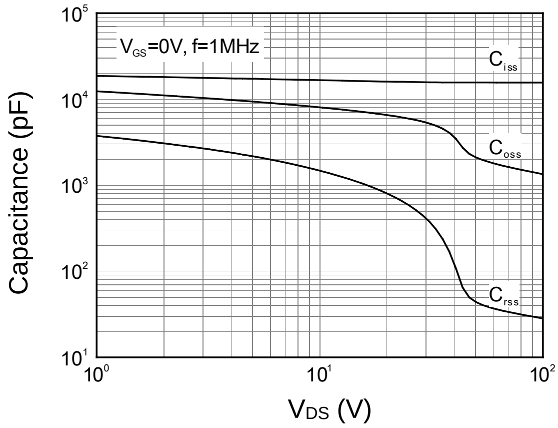


Figure 11. Capacitance

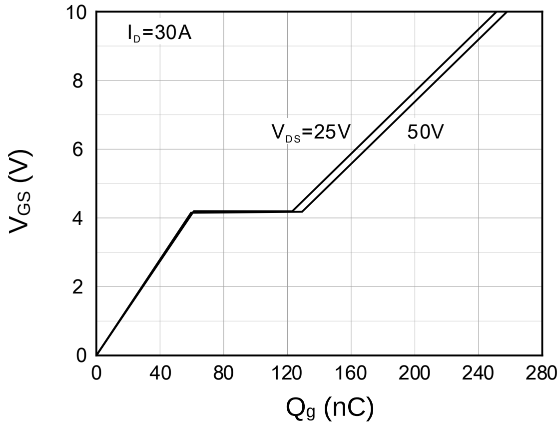
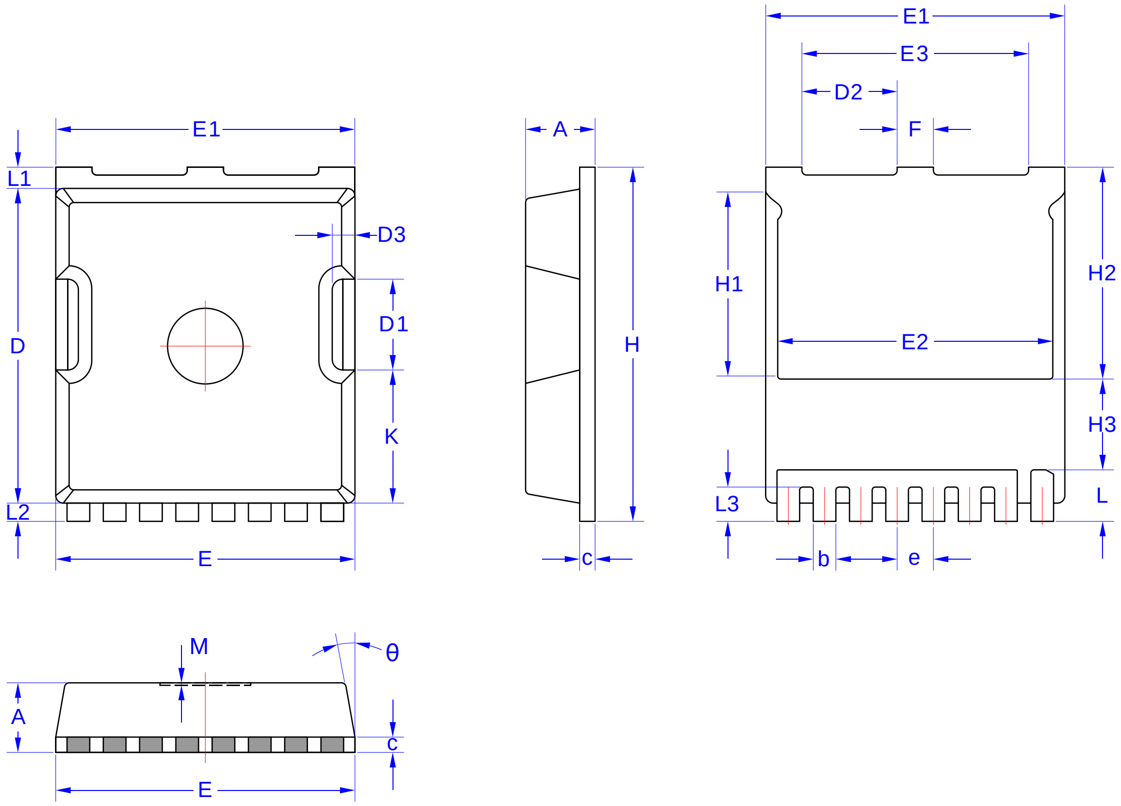


Figure 12. Gate charge

ckage Dimensions

TOLL-8L Package



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.65	0.75	0.85
c		0.508 REF	
D	10.25	10.40	10.55
D1	2.85	3.00	3.15
D2	2.95	3.10	3.25
D3		0.75 REF	
E	9.75	9.90	10.05
E1	9.65	9.80	9.95
E2	8.95	9.10	9.25
E3	7.25	7.40	7.55
e		1.20 BSC	

Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
F	1.05	1.20	1.35
H	11.55	11.70	11.85
H1	6.03	6.18	6.33
H2	6.85	7.00	7.15
H3		3.00 BSC	
K	4.25	4.40	4.55
L	1.55	1.70	1.85
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
M		0.08 REF	
θ	8°	10°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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