Dual P-Channel Enhancement Mode MOSFET

- **Features**

V_{DS} = -15V

I_D = -4.6A

$R_{DS(ON)}$

V_{GS}= -4.5V, TYP 47 mΩ

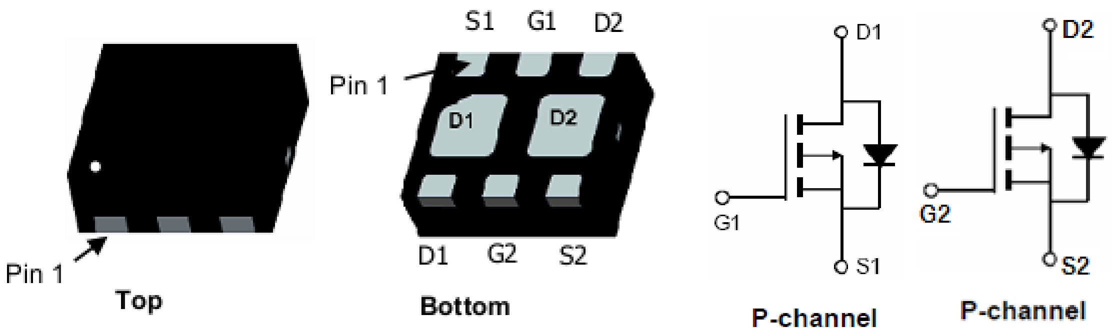
V_{GS}= -2.5V, TYP 61 mΩ

- **General Description**

• Power Management

• Portable Equipment

- **Pin Configurations**



DFN2*2-6L

- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

Parameter		**Symbol**	**Ratings**	**Unit**
Drain-Source Voltage		V_{DSS}	-15	V
Gate-Source Voltage		V_{GSS}	±10	V
Drain Current (Continuous) *AC	T_A=25°C	I_D	-4.6	A
	T_A=100°C		-2.9	
Drain Current (Pulse) *B		I_{DM}	-15	A
Power Dissipation	T_A=25°C	P_D	1.9	W
Operating Temperature/ Storage Temperature		T_J/T_{STG}	-55~150	℃

- **Thermal Resistance Ratings**

Parameter		**Symbol**	**Maximum**	**Unit**
Maximum Junction-to-Ambient	t ≤ 5 s	R_{thJA}	65	°C/W

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

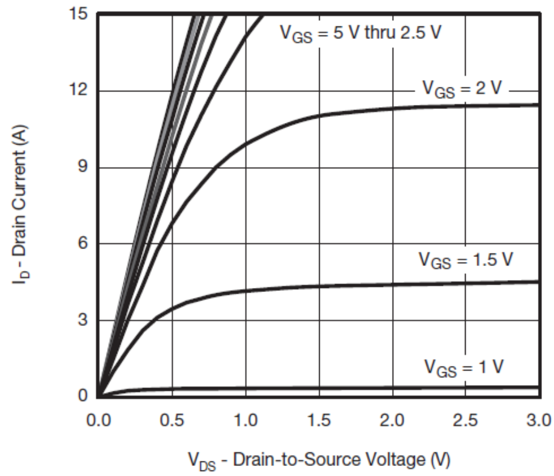
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D= -250μA	-15	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -15V, V_{GS} = 0V	--	--	-1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_{DS}= -250μA	-0.4	-0.62	-1	V
Gate Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V	--	--	±100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.8A	--	47	61	mΩ
	$R_{DS(on)}$	V_{GS} = -2.5V, I_D = -2A	--	61	80	mΩ
Diode Forward Voltage	V_{SD}	I_{SD}= -1A , V_{GS}=0V	--	-0.63	-1.2	V
Diode Forward Current *AC	I_S	T_A =25°C	--	--	-3	A
Switching						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 4.9 A	--	9.5	--	nC
Gate-Source Charge	Q_{gs}		--	1.4	--	nC
Gate-Drain Charge	Q_{gd}		--	2.3	--	nC
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 2.6Ω, I_D ≅ - 3.9 A, V_{GEN} = - 4.5 V, R_g = 1Ω	--	15	--	ns
Turn-on Rise Time	t_r		--	16	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	30	--	ns
Turn-Off Fall Time	t_f		--	10	--	ns
Dynamic						
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	--	781	--	pF
Output Capacitance	C_{oss}		--	98	--	pF
Reverse Transfer Capacitance	C_{rss}		--	96	--	pF

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

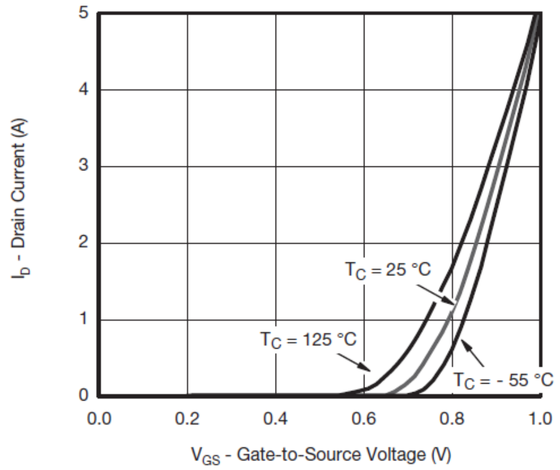
B: Repetitive rating, pulse width limited by junction temperature.

C: The current rating is based on the t≤ 10s junction to ambient thermal resistance rating,Package Limited -4.5A.

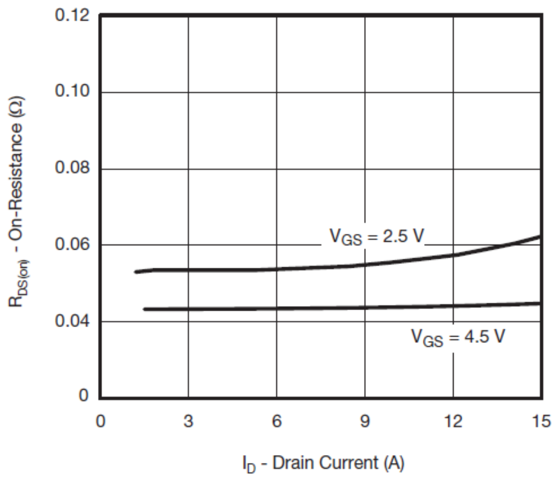
- **Typical Performance Characteristics（(TJ = 25 °C, unless otherwise noted)）**



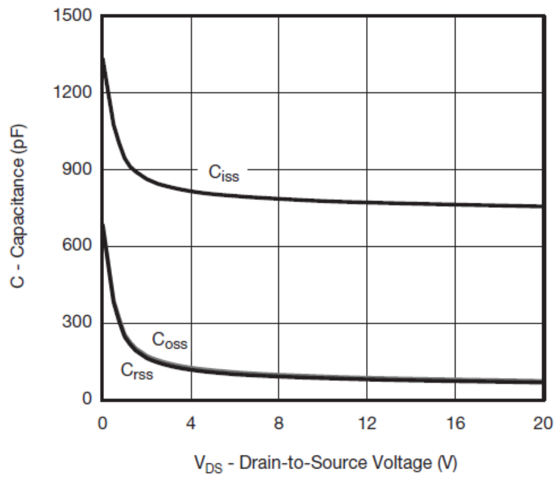
Output Characteristics



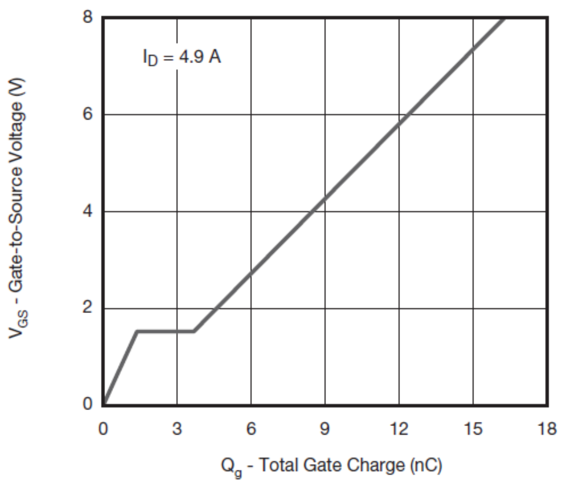
Transfer Characteristics



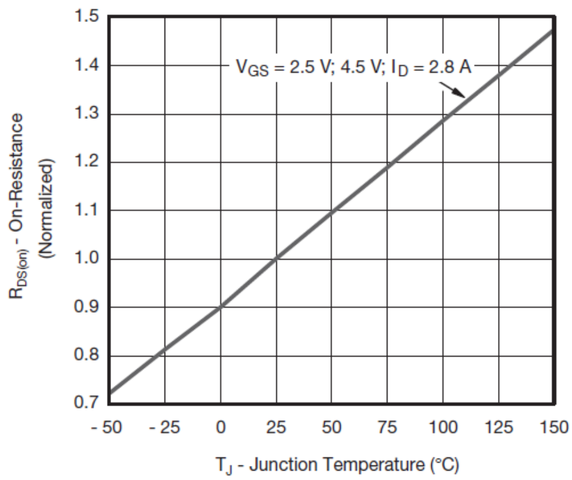
On-Resistance vs. Drain Current and Gate Voltage



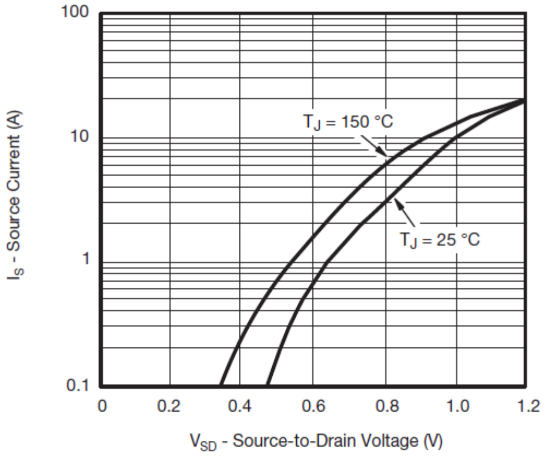
Capacitance



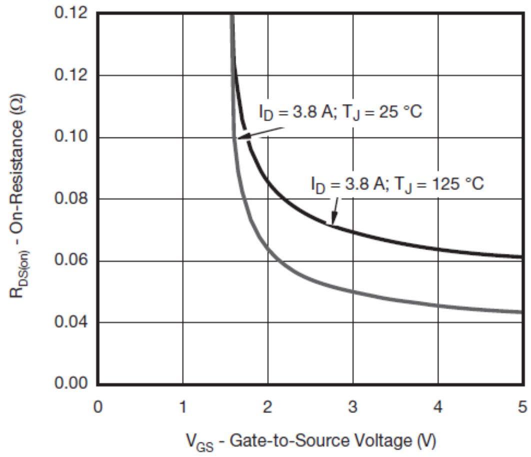
Gate Charge



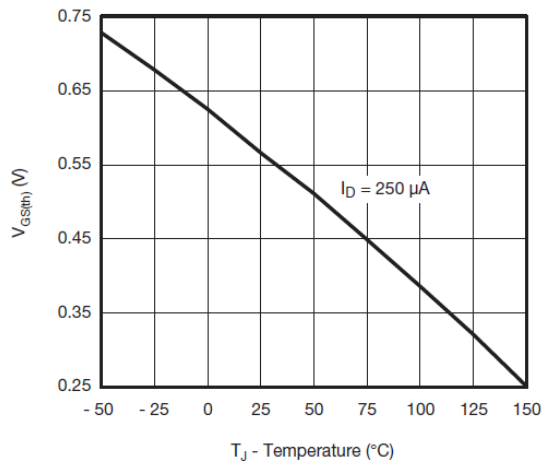
On-Resistance vs. Junction Temperature



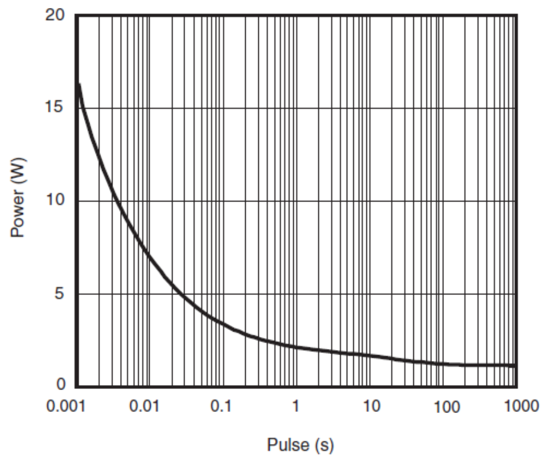
Source-Drain Diode Forward Voltage



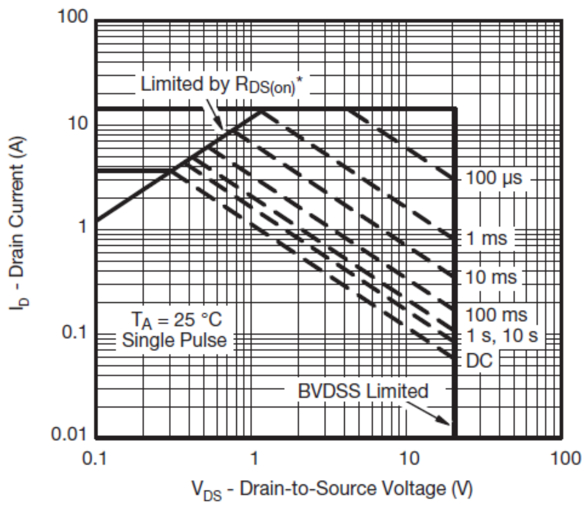
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



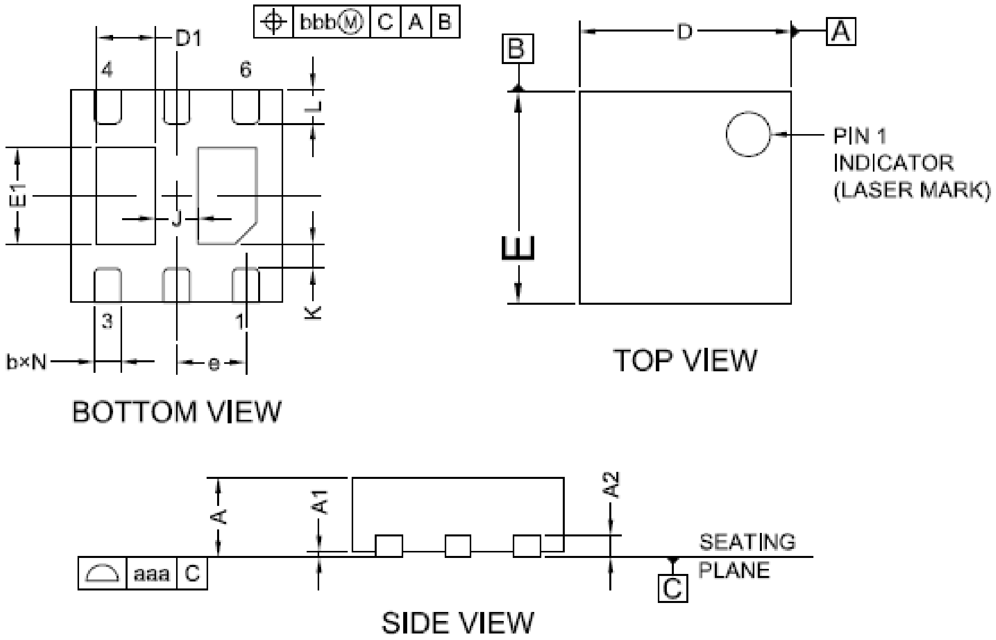
Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

- **Package Information**



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.225	0.275	0.325
D	1.95	2.00	2.05
D1	0.50	0.55	0.60
E	1.95	2.00	2.05
E1	0.85	0.90	0.95
e		0.65BSC	
L	0.27	0.32	0.37
J		0.40BSC	
K		0.20MIN	
N		6	
aaa		0.08	
bbb		0.10	

NOTES:

1.CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES).

2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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