

### Description

The XPX40NN10RD uses advanced technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 40A$

$R_{DS(ON)} < 14m\Omega$  @  $V_{GS}=10V$

### Application

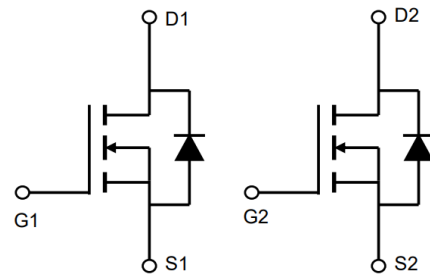
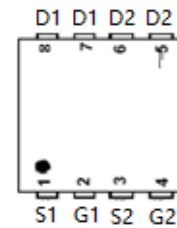
- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC

Marking and pin assignment



DFN5X6双基

Schematic Diagram



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX40NN10RD	PDFN5*6-8L	XPX40NN10RD XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain source voltage	100	V
VGS	Gate source voltage	$\pm 20$	V
ID	Continuous drain current <sup>1)</sup> , $T_C=25^\circ\text{C}$	40	A
ID, pulse	Pulsed drain current <sup>2)</sup> , $T_C=25^\circ\text{C}$	120	A
P <sub>D</sub>	Power dissipation <sup>3)</sup> , $T_C=25^\circ\text{C}$	71	W
EAS	Single pulsed avalanche energy <sup>5)</sup>	57	mJ
Tstg, T <sub>j</sub>	Operation and storage temperature	-55 to 150	$^\circ\text{C}$
R $\theta$ JC	Thermal resistance, junction-case	1.76	$^\circ\text{C/W}$
R $\theta$ JA	Thermal resistance, junction-ambient <sup>4)</sup>	25	$^\circ\text{C/W}$

**100V N+N-Channel Enhancement Mode MOSFET**
**Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BVDSS	Drain-source breakdown voltage	V <sub>GS</sub> =0 V, I <sub>D</sub> =250 μA	100	107		V
VGS(th)	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1.2	1.5	2.5	V
RDS(ON)	Drain-source on-state resistance	V <sub>GS</sub> =10 V, I <sub>D</sub> =10 A		14	20	mΩ
RDS(ON)	Drain-source on-state resistance	V <sub>GS</sub> =4.5 V, I <sub>D</sub> =7 A		18	25	mΩ
IGSS	Gate-source leakage current	V <sub>GS</sub> =±20 V			±100	nA
IDSS	Drain-source leakage current	V <sub>DS</sub> =100 V, V <sub>GS</sub> =0 V			1	uA
Ciss	Input capacitance	V <sub>GS</sub> =0 V, V <sub>DS</sub> =50 V, f=100 kHz		1013.9		pF
Coss	Output capacitance			185.4		pF
Crss	Reverse transfer capacitance			9.8		pF
td(on)	Turn-on delay time	V <sub>GS</sub> =10 V, V <sub>DS</sub> =50 V, R <sub>G</sub> =10 Ω, I <sub>D</sub> =5 A		16.6		ns
t <sub>r</sub>	Rise time			3.8		ns
td(off)	Turn-off delay time			75.5		ns
t <sub>f</sub>	Fall time			46		ns
Q <sub>g</sub>	Total gate charge	I <sub>D</sub> =5 A, V <sub>DS</sub> =50V, V <sub>GS</sub> =10V		16.2		nc
Q <sub>gs</sub>	Gate-source charge			2.8		nc
Q <sub>gd</sub>	Gate-drain charge			4.1		nc
V <sub>plateau</sub>	Gate plateau voltage			3		V
I <sub>S</sub>	Diode forward current	V <sub>GS</sub> <V <sub>th</sub>		30		A
I <sub>SP</sub>	Pulsed source current			90		A
t <sub>rr</sub>	Reverse recovery time	I <sub>S</sub> =1A, di/dt=100 A/μs	49			ns
Q <sub>rr</sub>	Reverse recovery charge		61.8			nc
I <sub>rrm</sub>	Peak reverse recovery current		2.4			A

**Note :**

1. Calculated continuous current based on maximum allowable junction temperature.
2. Repetitive rating; pulse width limited by max. junction temperature.
3. Pd is based on max. junction temperature, using junction-case thermal resistance.
4. The value of R<sub>Θja</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>a</sub>=25 °C.
5. V<sub>DD</sub>=50 V, R<sub>G</sub>=25 Ω, L=0.3 mH, starting T<sub>J</sub>=25 °C.

### Typical Characteristics

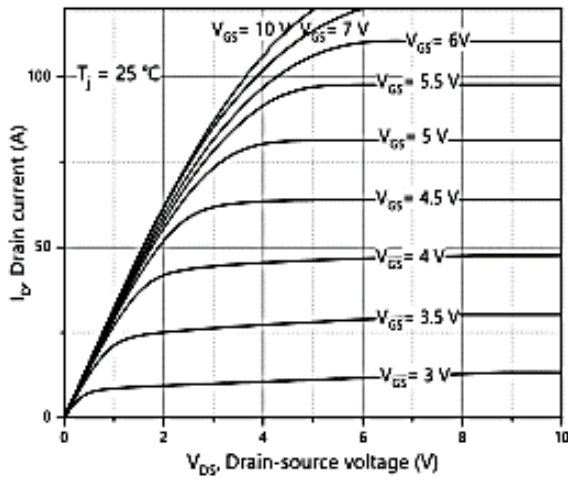


Figure 1, Typ. output characteristics

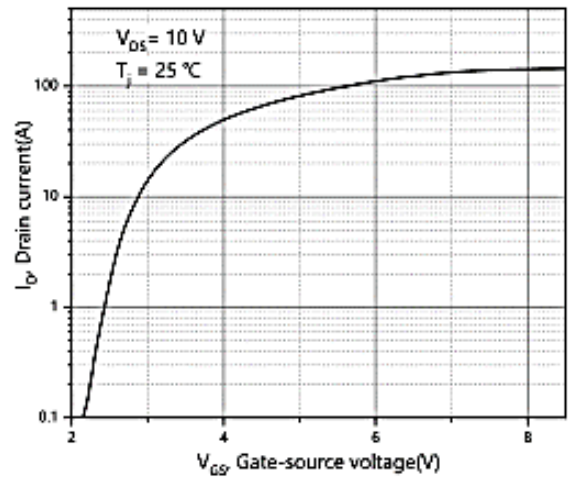


Figure 2, Typ. transfer characteristics

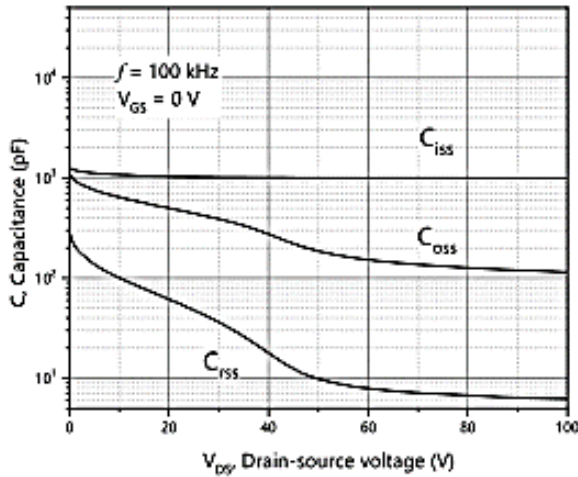


Figure 3, Typ. capacitances

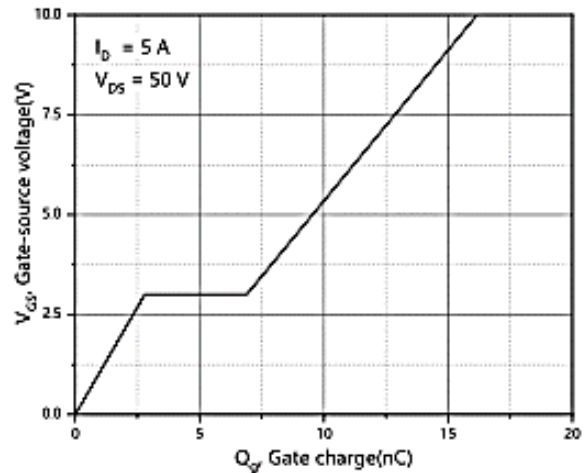


Figure 4, Typ. gate charge

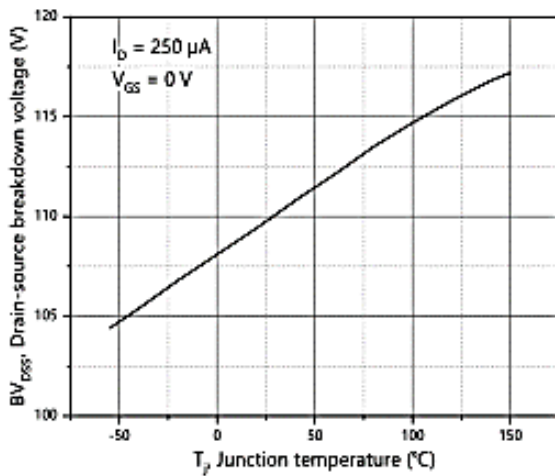


Figure 5, Drain-source breakdown voltage

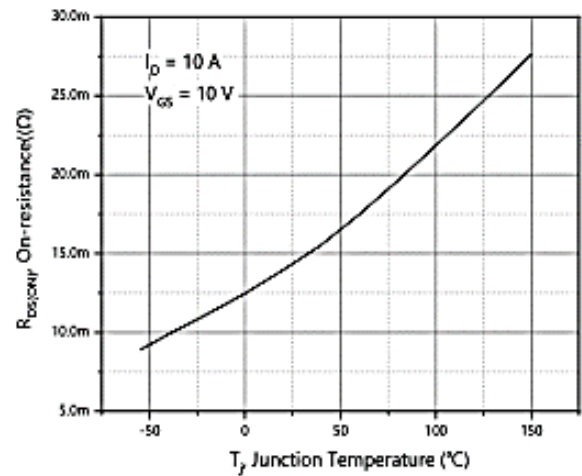


Figure 6, Drain-source on-state resistance

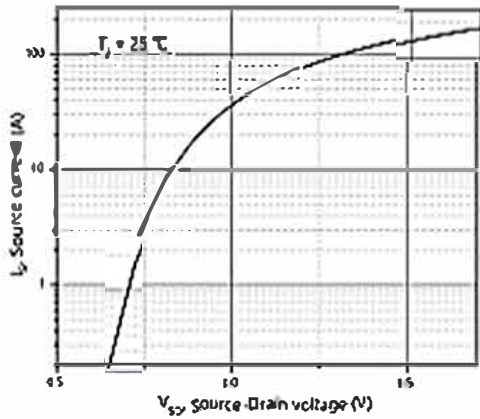


Figure 7. Forward characteristic of body diode

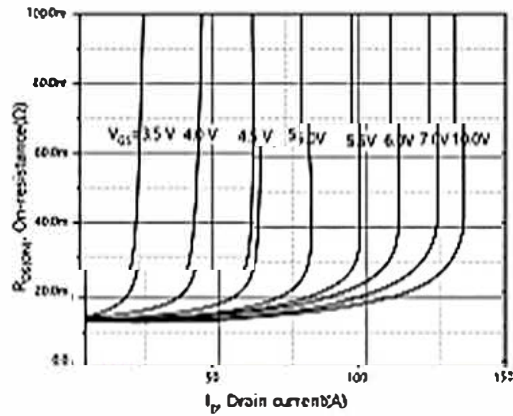


Figure 8. Drain-source on-state resistance

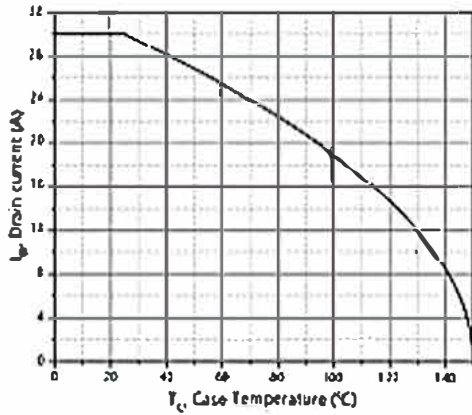


Figure 9. Drain current

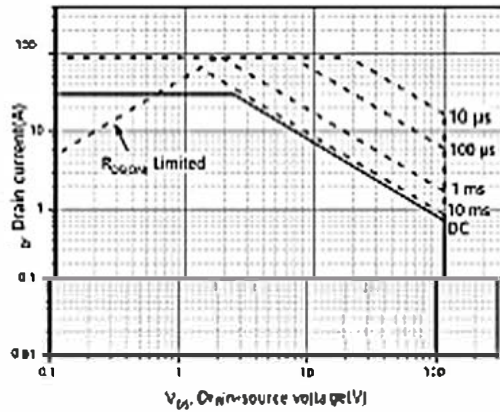


Figure 10. Safe operation area  $T_C=25\text{ }^\circ\text{C}$

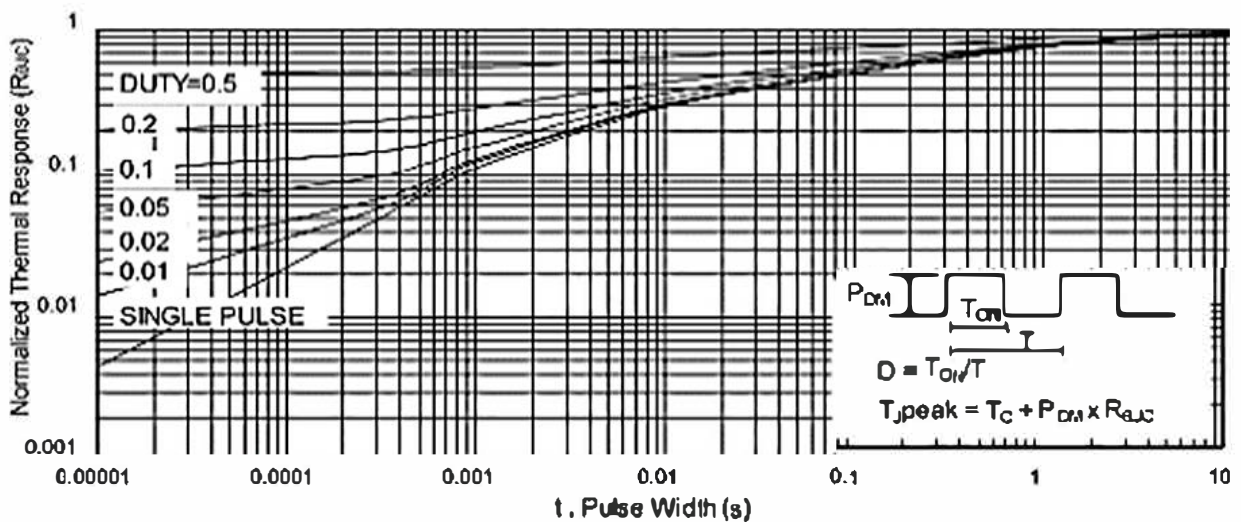
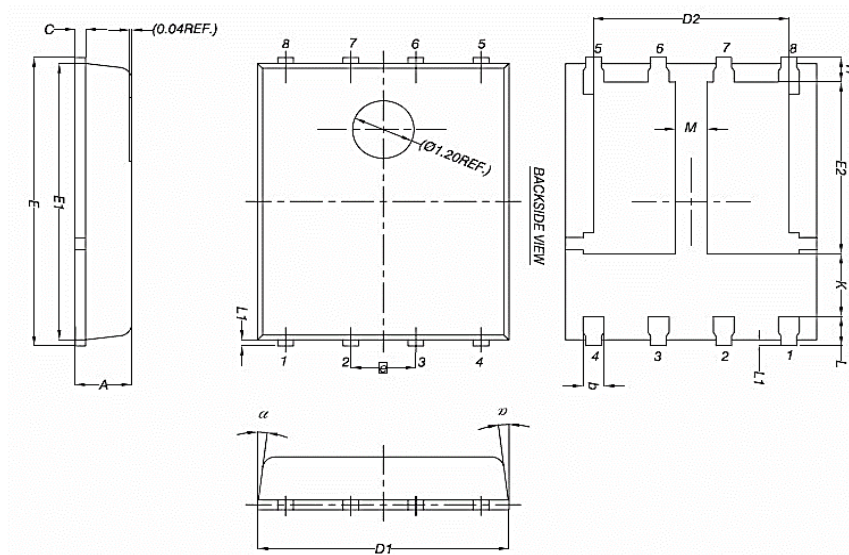


Figure 11. Normalized Maximum Transient Thermal Impedance

**Package Mechanical Data-DFN5\*6-8L-JQ Double**


Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	3.30	3.45
E2	3.38	3.05	3.20
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°

## 100V N+N-Channel Enhancement Mode MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1 sec
Pb-Free device	260°C +0/-5°C	5sec ±1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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