40V N-Channel Enhancement Mode Power MOSFET

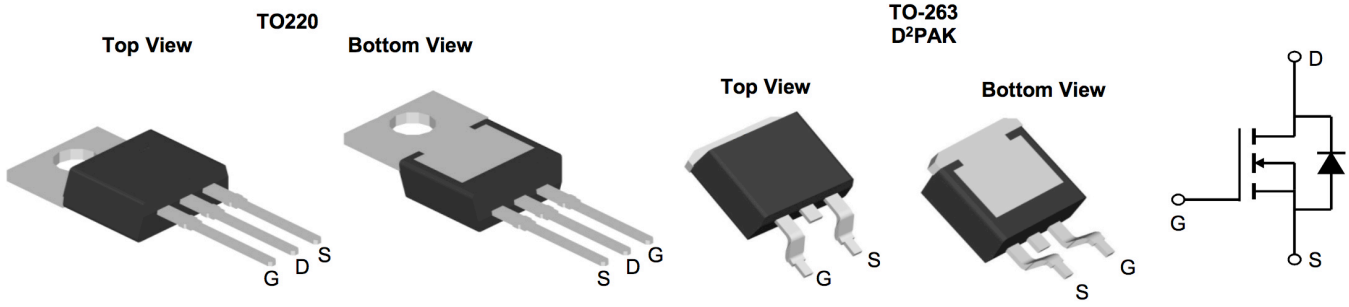
Features

- 40V/190A,
  $R_{DS\ (ON)}$ =1.8mΩ(Typ.)@V_{GS}=10V
- 100% avalanche testedh t t d
- 175°C Operating Temperatur
- Lead Free and Green Devices Available (RoHS Compliant

- Motor Drive
- Uninterruptible Power Supplie
- DC/DC converte
- General Purpose Application

Pb-Free RoHS HF Halogen-Free

- **Pin Configurations**



Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
Common Ratings (T_C=25°C Unless Otherwise Noted)				
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		175	°C
T_{STG}	Storage Temperature Range		-55 to 175	°C
I_S	Diode Continuous Forward Current	T_C=25°C	190	A
Mounted on Large Heat Sink				
I_{DP} ①	300μs Pulse Drain Current Tested	T_C=25°C	760	A
I_D ②	Continuous Drain Current(V_{GS}=10V)	T_C=25°C	190	A
		T_C=100°C	146	
P_D	Maximum Power Dissipation	T_C=25°C	300	W
		T_C=100°C	150	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		0.5	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5	°C/W
Drain-Source Avalanche Ratings				
E_{AS} ③	Avalanche Energy, Single Pulsed		812	mJ

Electrical Characteristics (T_C=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Condition	XPX40190TU			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
		T_J=125°C			30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	2		4	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
$R_{DS(ON)}$ ④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=75A		1.8	3	mΩ
Diode Characteristics						
V_{SD} ④	Diode Forward Voltage	I_{SD}=75A, V_{GS}=0V			1.3	V
t_{rr}	Reverse Recovery Time	I_{SD}=75A, dI_{SD}/dt=100A/μs		40		ns
Q_{rr}	Reverse Recovery Charge			52		nC
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,F=1MHz		1.2		Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, Frequency=1.0MHz		4800		pF
C_{oss}	Output Capacitance			950		
C_{rss}	Reverse Transfer Capacitance			480		
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=20V,I_{DS}=75A, V_{GEN}=10V,R_G=2.5Ω		19		ns
t_r	Turn-on Rise Time			96		
$t_{d(OFF)}$	Turn-off Delay Time			70		
t_f	Turn-off Fall Time			50		
Gate Charge Characteristics ⑤						
Q_g	Total Gate Charge	V_{DS}=32V, V_{GS}=10V, I_{DS}=75A		120		nC
Q_{gs}	Gate-Source Charge			34		
Q_{gd}	Gate-Drain Charge			46		

Notes:

①Pulse width limited by safe operating area.

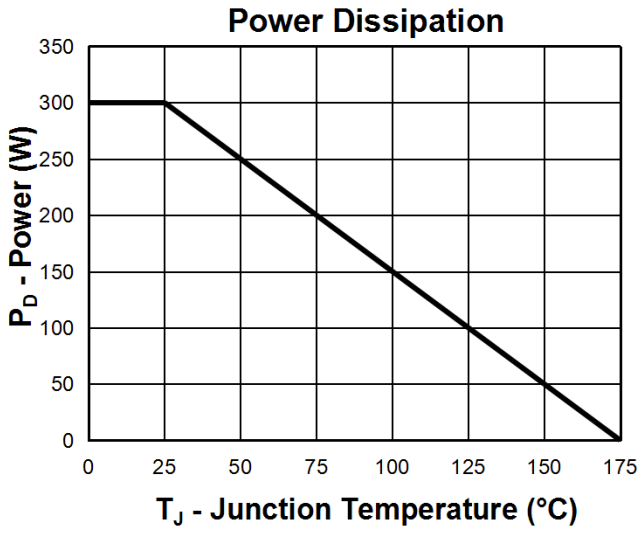
②Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A.

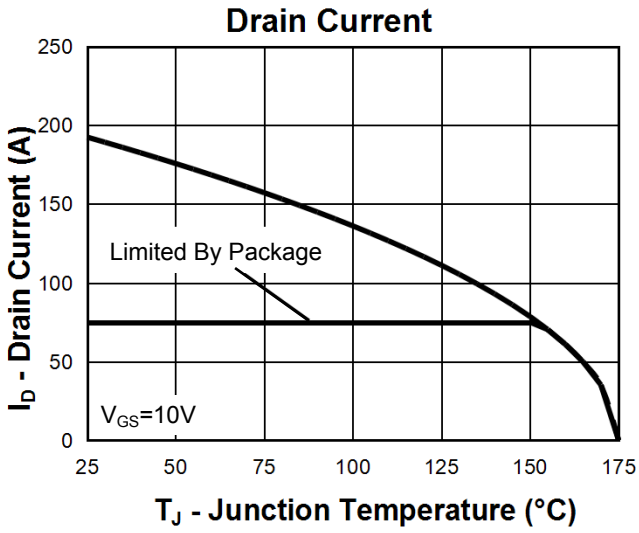
③Limited by T_{Jmax}, I_{AS} =57A, V_{DD} = 32V, R_G = 50Ω , Starting T_J = 25°C.

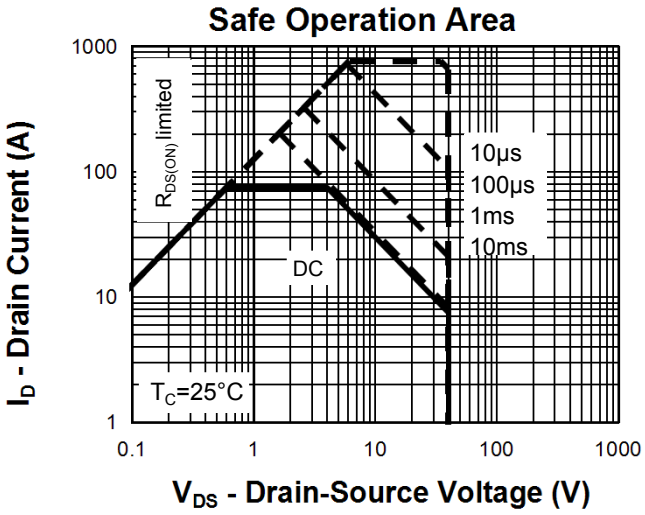
④Pulse test ; Pulse width≤300μs, duty cycle≤2%.

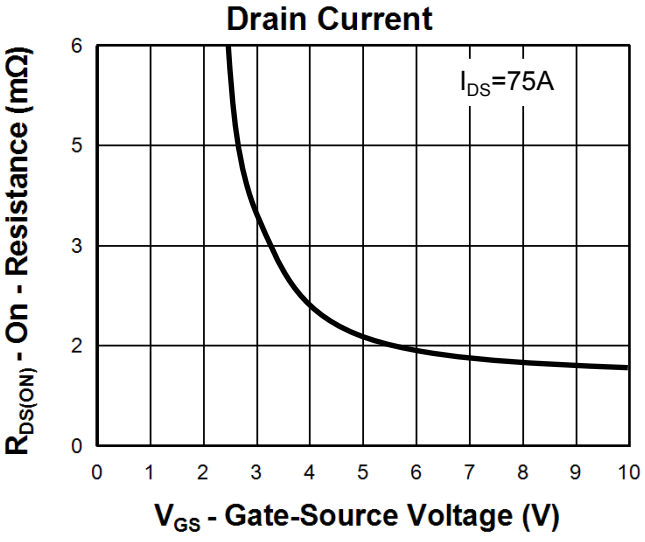
⑤Guaranteed by design, not subject to production testing.

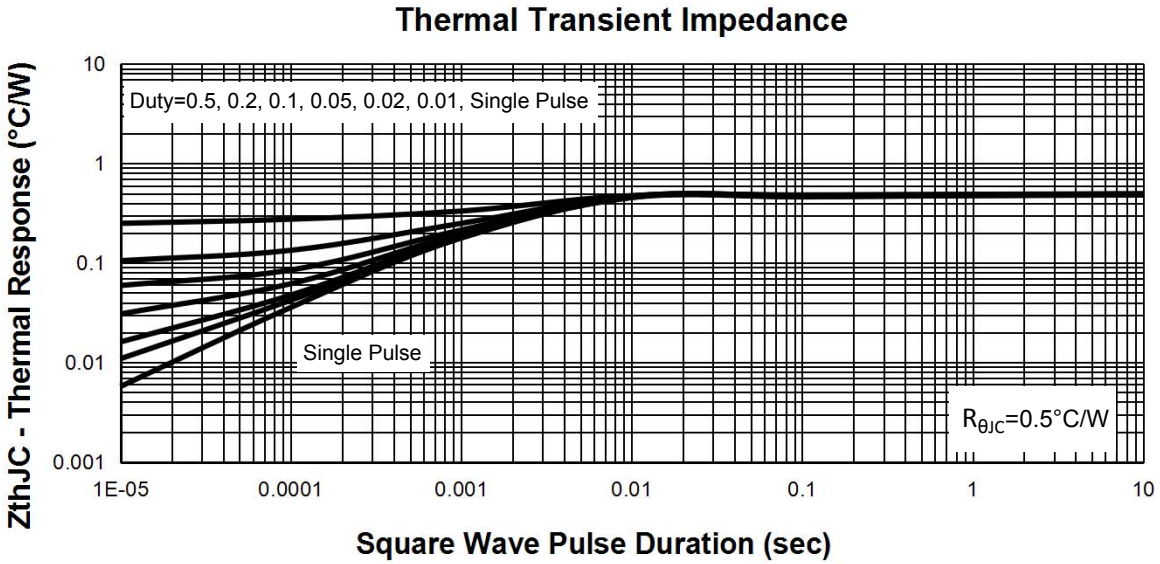
Typical Characteristics





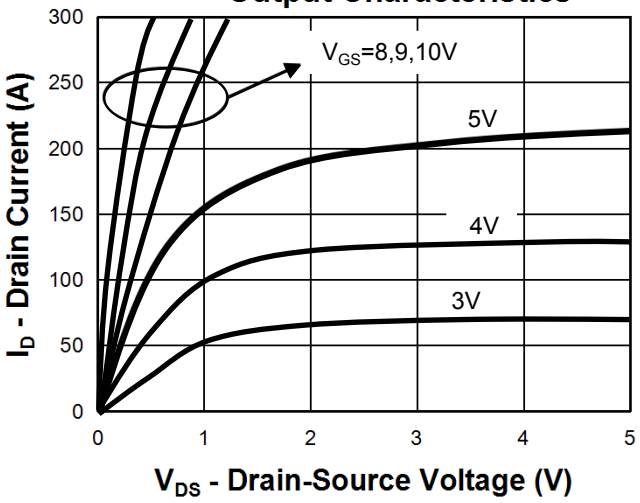




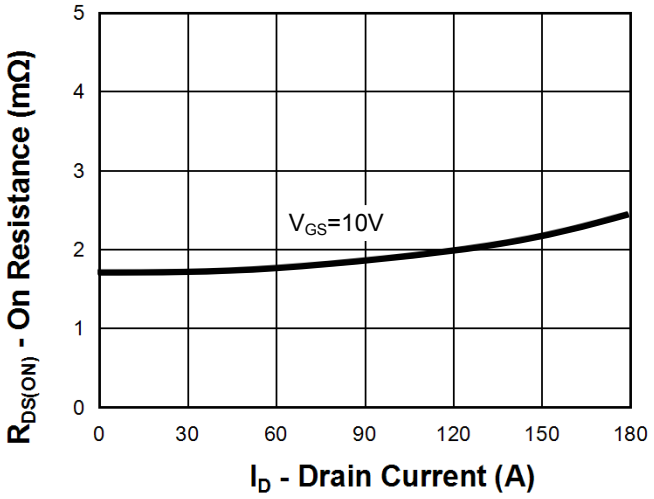


Typical Characteristics

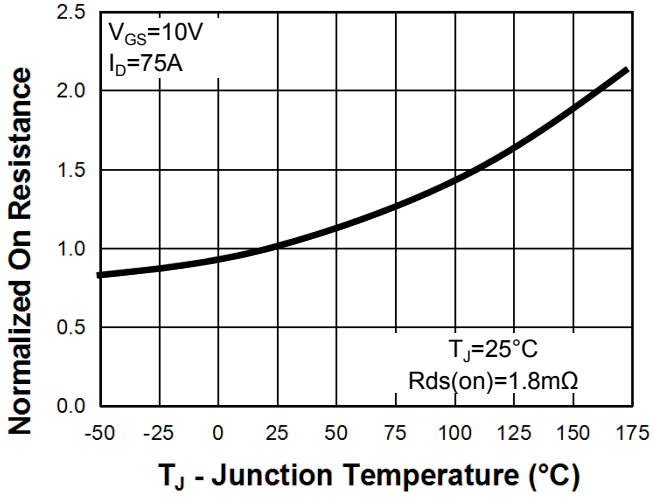
Output Characteristics



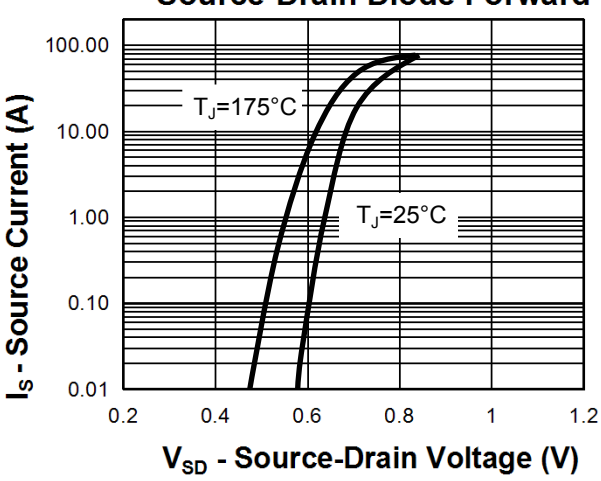
Drain-Source On Resistance



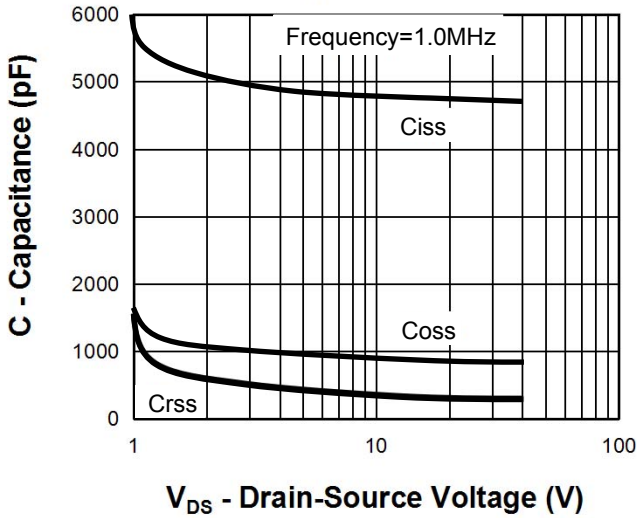
Drain-Source On Resistance



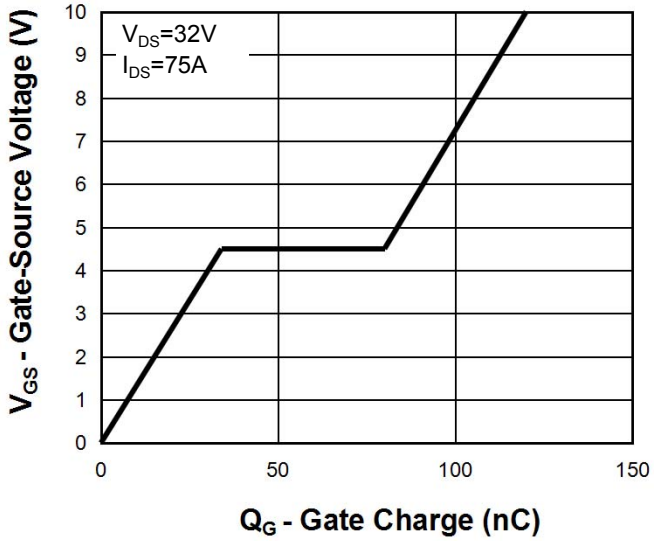
Source-Drain Diode Forward



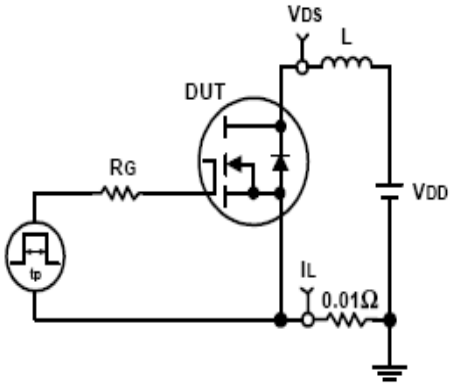
Capacitance

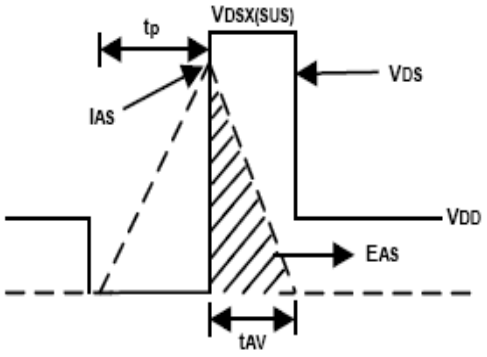


Gate Charge

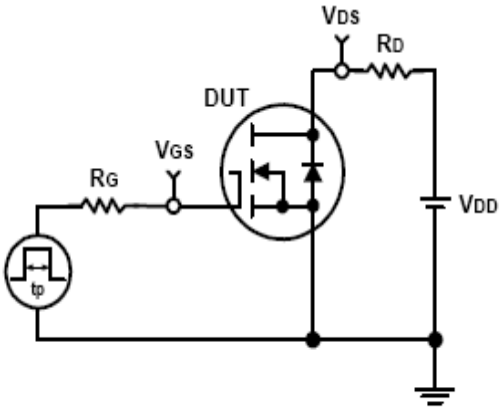


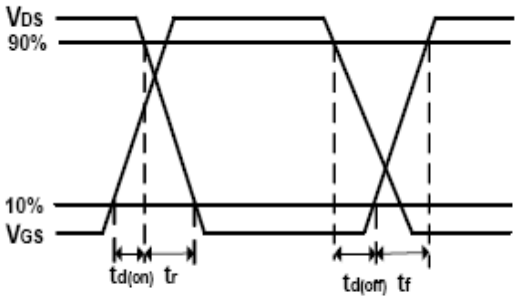
Avalanche Test Circuit and Waveforms





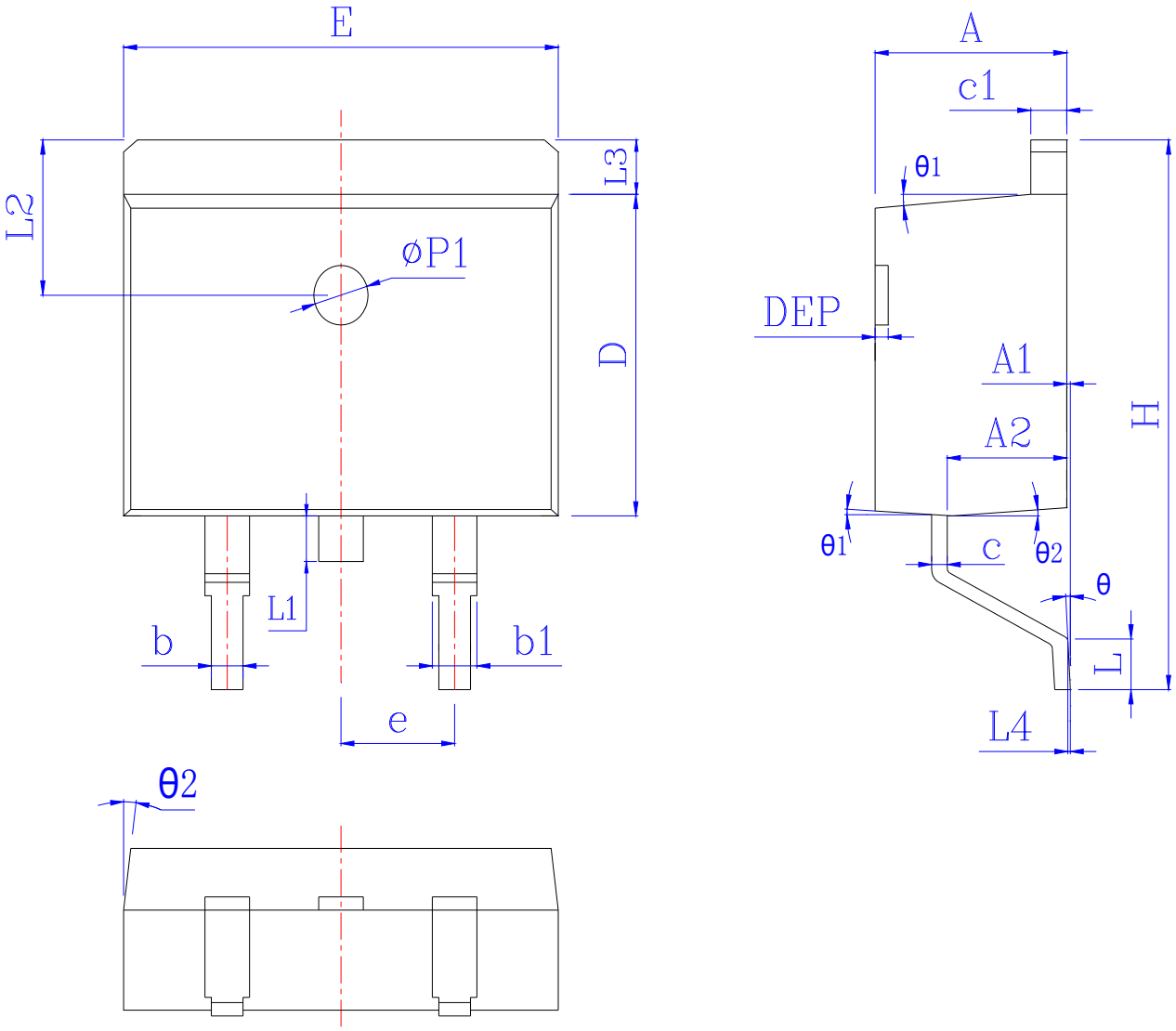
Switching Time Test Circuit and Waveforms





Package Information

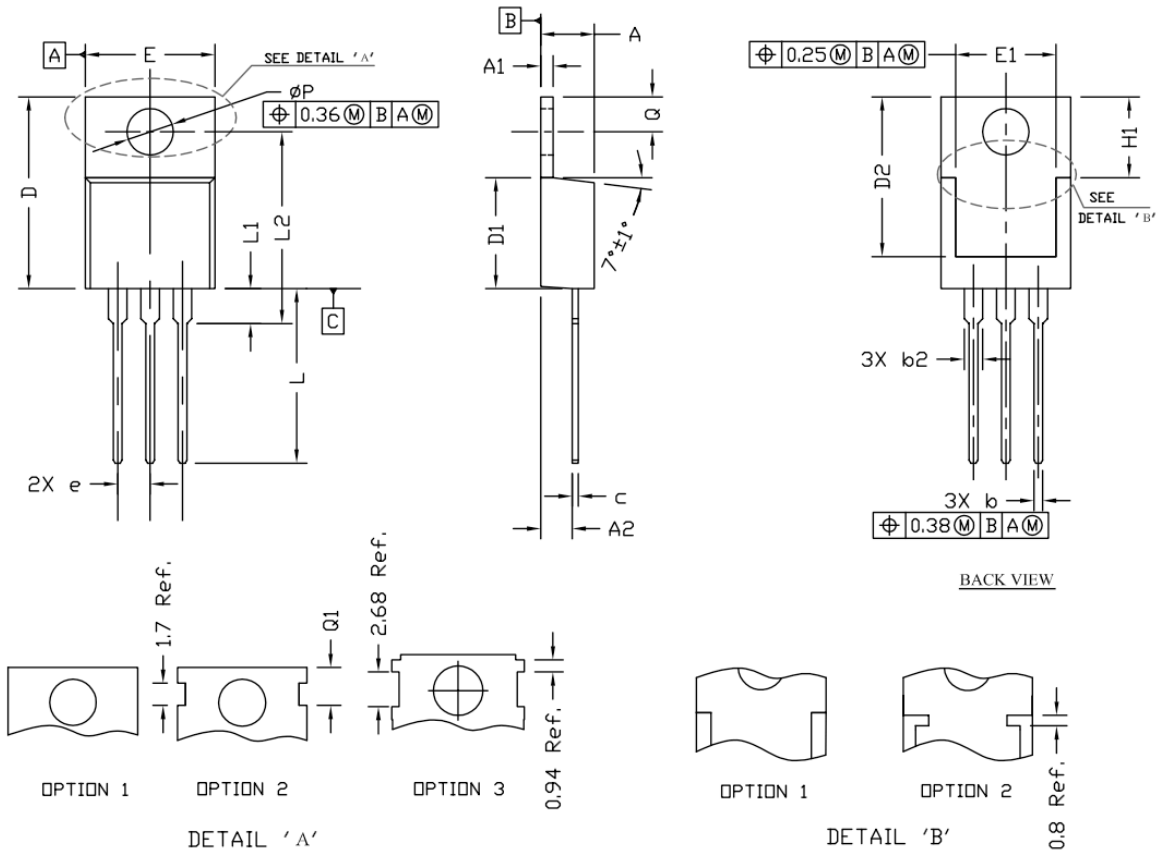
TO263



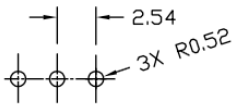
SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.55	4.72	0.173	0.179	0.186	L	1.94	2.30	2.60	0.076	0.091	0.102
A1	0.00	0.10	0.25	0.000	0.005	0.010	L3	1.17	1.29	1.40	0.046	0.051	0.055
A2	2.59	2.69	2.79	0.102	0.106	0.110	L1	*	*	1.70	*	*	0.067
b	0.76	*	0.90	0.030	*	0.035	L4	0.25 BSC			0.01 BSC		
b1	1.22	*	1.36	0.048	*	0.054	L2	2.50 REF			0.098 REF		
c	0.33	*	0.47	0.013	*	0.019	θ	0°	*	8°	0°	*	8°
c1	1.22	*	1.32	0.048	*	0.052	θ1	5°	7°	9°	5°	7°	9°
D	8.60	*	9.29	0.339	*	0.366	θ2	1°	3°	5°	1°	3°	5°
E	9.95	*	10.26	0.392	*	0.404	DEP	0.05	0.10	0.20	0.002	0.004	0.008
e	2.54BSC			0.100BSC			Φp1	1.40	1.50	1.60	0.055	0.059	0.063
H	14.70	15.10	15.79	0.579	0.594	0.622							

- **Package Information**

TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN



UNIT: mm

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC.		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
øP	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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