150V N-ChannelEnhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX270N15LL uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

V_{DS} =150V,I_D =270A

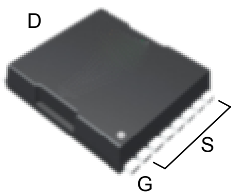
$R_{DS(ON)}$=4.6mΩ (typ) @ V_{GS}=10V

General Features

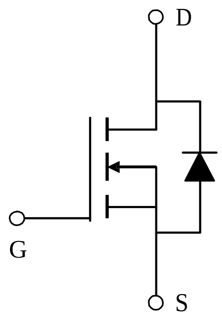
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching



TO-LL



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX270N15LL	TOLLA-8L	XPX270N15LL XXX YYYY	2000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	150	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V	260	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V	185	A
IDM	Pulsed Drain Current	740	A
EAS	Single Pulse Avalanche Energy	1764	mJ
IAS	Avalanche Current	64	A
P_D@T_C=25℃	Total Power Dissipation[4]	326	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient	0.46	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case	40	℃/W

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Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	150	165		V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=140V, V_{GS}=0V			1	μA
IGSS	Gate-Body Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	2.0	2.9	4.0	V
GFS	Forward Transconductance	V_{DS}=5V, I_D=15A		33		S
RDS(ON)	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A		4.6	5.8	mΩ
Ciss	Input Capacitance	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		4100		pF
Coss	Output Capacitance			2867		pF
Crss	Reverse Transfer Capacitance			215		pF
td(on)	Turn-on Delay Time	V_{GS}=10V, V_{DS}=75V, RL=1.07Ω, RGEN=3Ω		18		nS
tr	Turn-on Rise Time			22		nS
td(off)	Turn-Off Delay Time			35		nS
t_f	Turn-Off Fall Time			10		nS
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=75V, I_D=70A		65		nC
Qgs	Gate-Source Charge			20		nC
Qgd	Gate-Drain Charge			19		nC
ISD	Source-Drain Current (Body Diode)				240	A
VSD	Forward on Voltage (Note 3)	V_{GS}=0V, I_S=20A			1.2	V
trr	Reverse Recovery Time	I_F=20A, dI/dt=500A/us		101		ns
Qrr	Reverse Recovery Charge	I_F=20A, dI/dt=500A/us		1,240		nC

Notes:

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3、The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=64A
4、The power dissipation is limited by 150°C junction temperature
5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

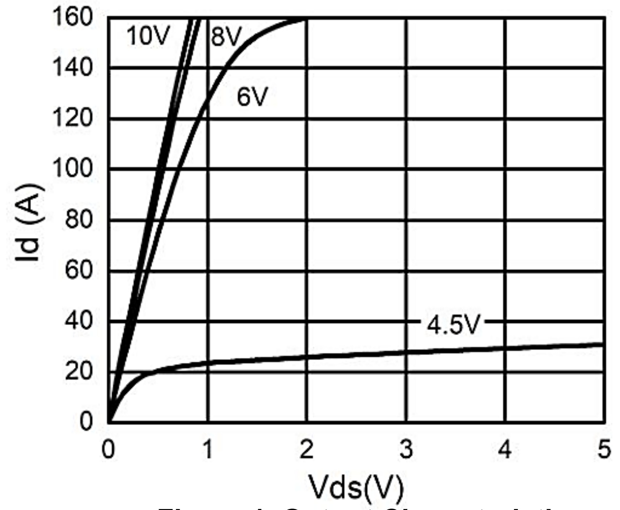

Figure 1. Output Characteristics

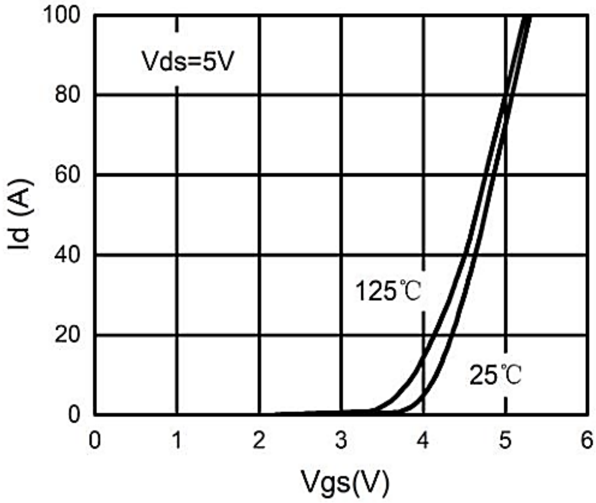

Figure 2. Transfer Characteristics

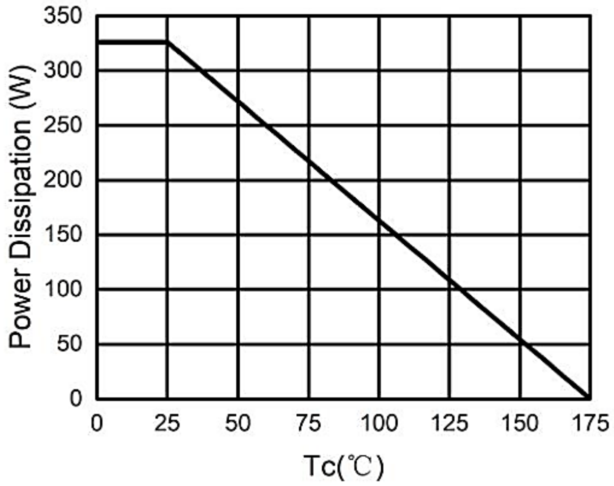

Figure 3. Power Dissipation

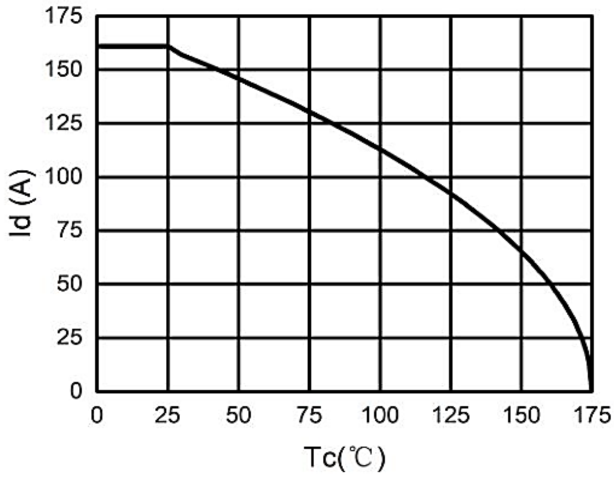

Figure 4. Drain Current

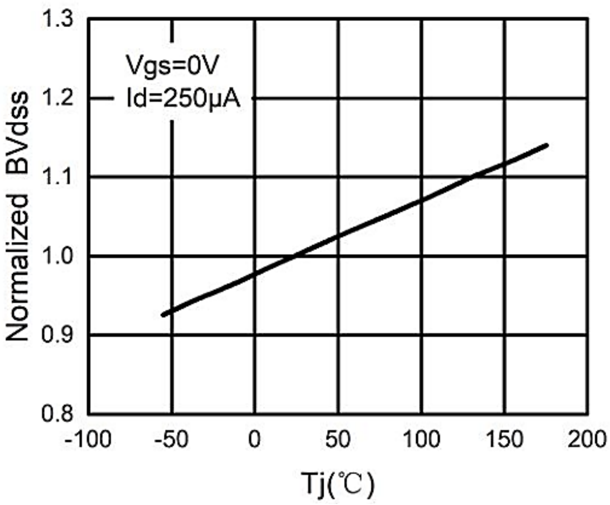

Figure5. BVDSS vs Junction Temperature

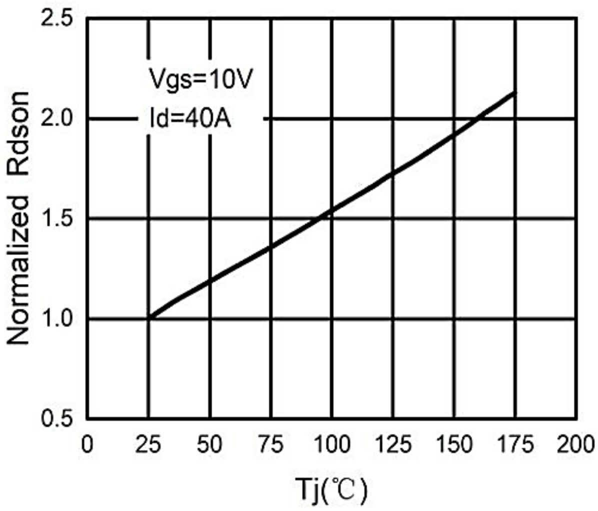

Figure6. RDS(ON) vs Junction Temperature

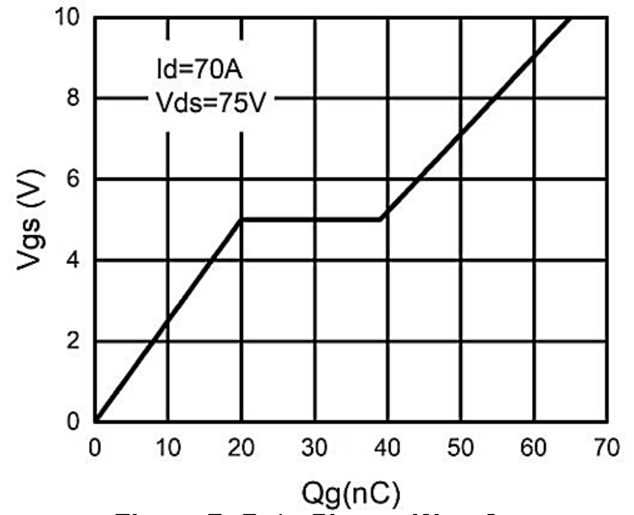

Figure 7. Gate Charge Waveforms

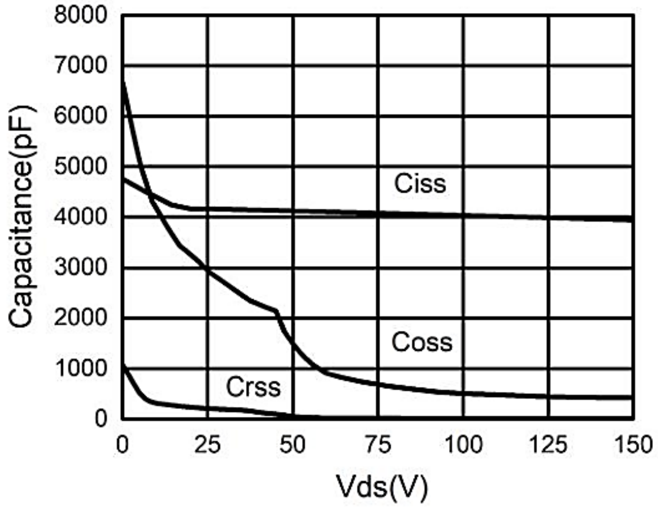

Figure 8. Capacitance

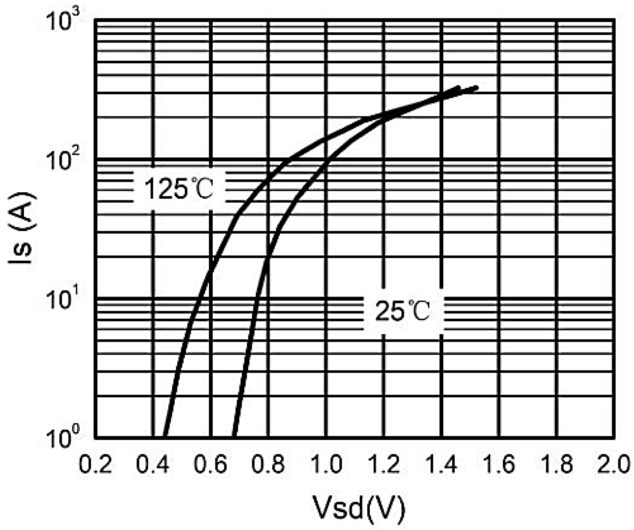

Figure 9. Body-Diode Characteristics

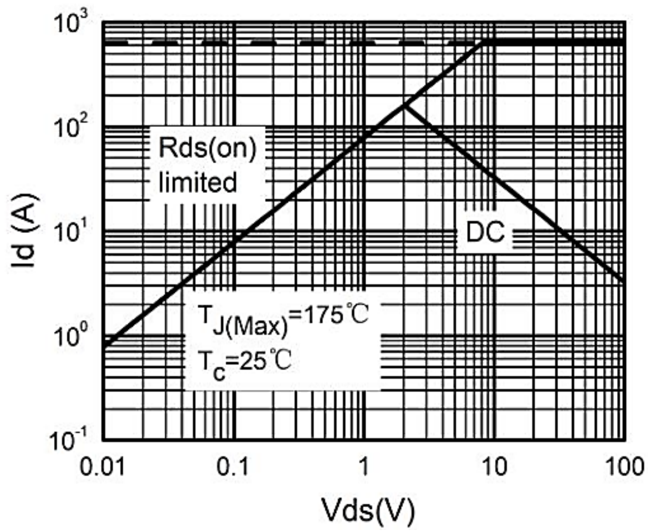

Figure 10. Maximum Safe Operating Area

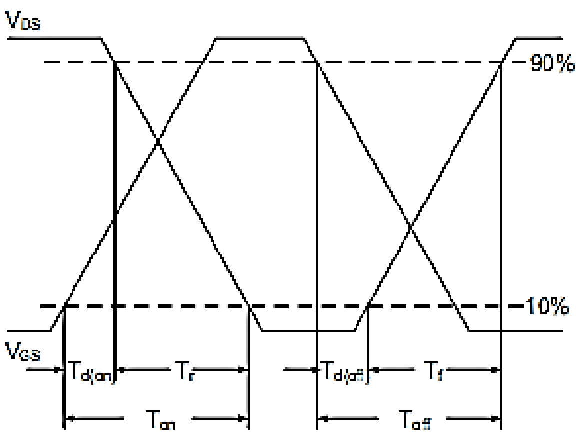

Figure11.Switching Time Waveform

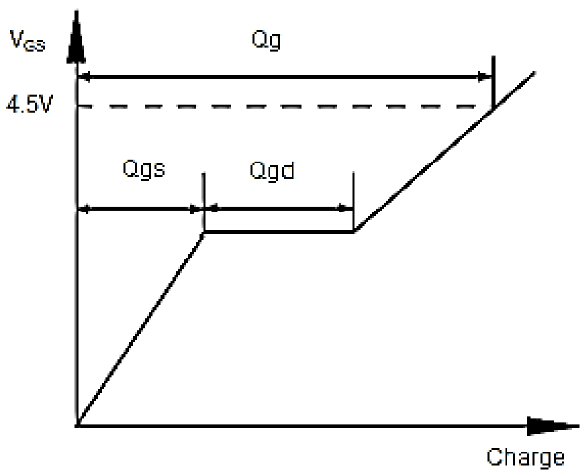

Figure12.Gate Charge Waveform

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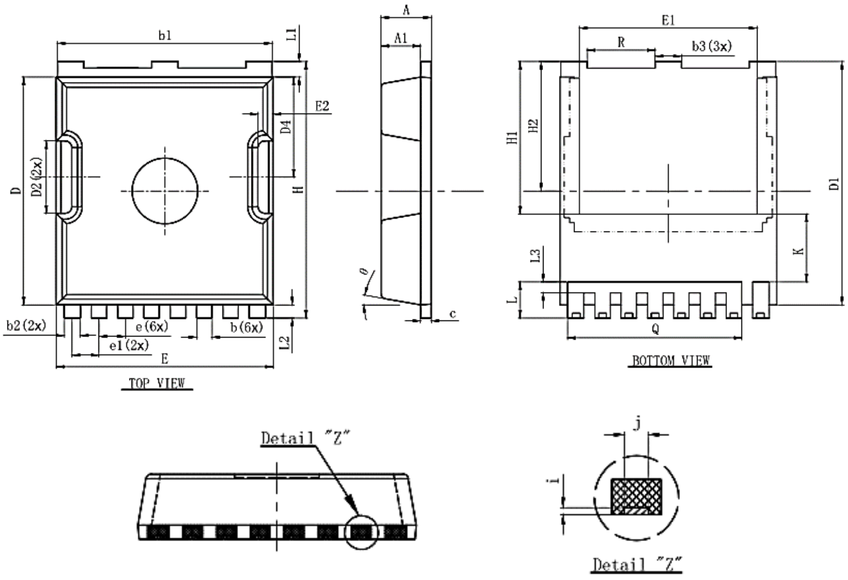
Package Mechanical Data-TOLLA-8-XZ Single



Symbol	Dimensions In Millimeters		
	Min.	Nom	Max.
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.6	0.7	0.8
b1	9.7	9.8	9.9
b2	0.65	0.75	0.85
b3	1.1	1.2	1.3
C	0.4	0.5	0.6
D	10.3	10.4	10.5
D1	11.0	11.1	11.2
D2	3.2	3.3	3.4
D4	4.47	4.57	4.67
E	9.8	9.9	10.0
E1	8.0	8.1	8.2
E2	0.5	0.6	0.7
e	1.200（BSC）		
e1	1.225（BSC）		
H	11.6	11.7	11.8
H1	6.95BSC		
H2	5.9BSC		
i	0.1REF		
j	0.350REF		
K	3.100REF		
L	1.55	1.65	1.75
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.4	0.5	0.6
Q	7.95REF		
R	3.0	3.1	3.2
θ	10°REG		

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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