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Halogen-Free

500V N-Channel Enhancement Mode MOSFET

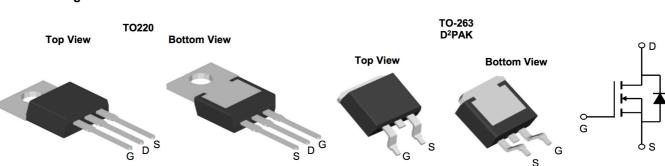
Features

- 500V/18A, $R_{DS (ON)}$ =340m $\Omega(Typ.)@V_{GS}$ =10V
- 100% avalanche testedh t t d
- 175°C Operating Temperatur

RoHS

Lead Free and Green Devices Available (RoHS Compliant

- Motor Drive
- Uninterruptible Power Supplie
- DC/DC converte
- General Purpose Application
- Pin Configurations



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX18N50TU	TO-263-3	XPX18N50TU XXX YYYY	800

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V _{GS} = 0V)	500	V
ID	Continuous Drain Current	18	А
IDM	Pulsed Drain Current (note1)	58	A
VGS	Gate-Source Voltage	±30	V
Eas	Single Pulse Avalanche Energy (note2)	452	mJ
IAR	Avalanche Current (note1)	14	А
Ear	Repetitive Avalanche Energy note1)	60	mJ
PD	Power Dissipation (T _c = 25°C)	32	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	°C
RthJC	Thermal Resistance, Junction-to-Case	4.12	°C/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	°C/W



Electrical Characteristics (TJ=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Мах	Units
BVDSS	Drain-Source Breakdown Voltage	VGS = 0 V, ID = 250 µA	500	550		V
ΔBVDSS/ ΔTJ	Breakdown Voltage Temperature Coefficient	ID = 250 µA, Referenc ed to 25°C		0.52		V/°C
1000		VDS=500 V, VGS=0V			1	μA
IDSS	Zero Gate Voltage Drain Current	VDS=400 V, TC=125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	VGS= 30V, VDS=0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	VGS=-30 V, VDS=0V			-100	nA
VGS(TH)	Gate Threshold voltage	VDS=VGS, ID=250 uA	2.0	3.0	4.0	V
RDS(On)	Drain-Source on-state resistance	VGS=10V, ID = 6.5A, TJ = 25°C		340	400	mΩ
gFS	Forward Transconductance	VDS = 40 V, ID=6.5A (Note 4)		12.8		S
Ciss	Input capacitance			1651		pF
Coss	Output capacitance	VDS=25V, VGS=0V, f=1.0MHz		188		pF
Crss	Reverse transfer capacitance			7		pF
td(on)	Turn On Delay Time			31		ns
tr	Rising Time	VDD= 250 V, ID =16 A,		43		ns
td(off)	Turn Off Delay Time	RG = 25 Ω		106		ns
tf	Fall Time	-		46		ns
Qg	Total Gate Charge			23.5		nC
Qgs	Gate-Source Charge	VDS = 400 V, ID = 13 A, VGS = 10 V		6.9		nC
Qgd	Gate-Drain Charge	VG3 - 10 V		7.4		nC
ISM	Maximum Pulsed Drain-Sou	n-Source Diode Forward Current			52	Α
VSD	Diode Forward Voltage	VGS= 0 V, IS = 13 A			1.2	V
trr	Reverse Recovery Time	VGS = 0 V, IS = 13 A, dIF / dt = 100		340		ns
Qrr	Reverse Recovery Charge	A/µs Note 4)		2.8		μC

Note :

 $1_{\mbox{\tiny V}}$ The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=4.1Mh $\,$ IAS=14A, VDD=50V, RG=25\Omega, Starting TJ = 25 ^{o}C

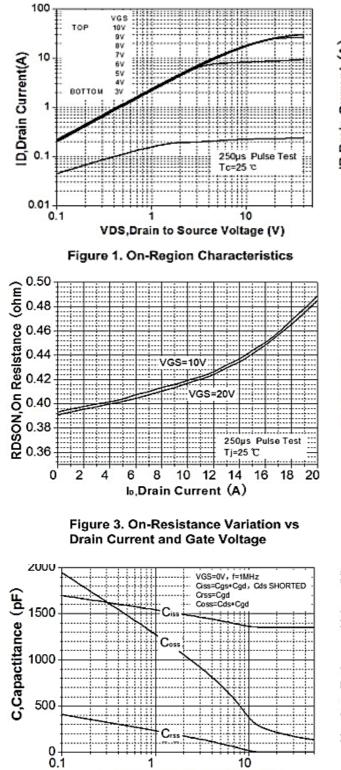
3、The test condition is Pulse Test: Pulse width \leq 300µs, Duty Cycle \leq 1%

4. The power dissipation is limited by 150 $^\circ\!\mathrm{C}$ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

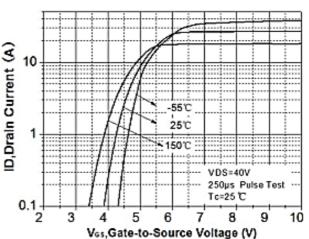






Vps,Drain-to-Source Voltage (V)







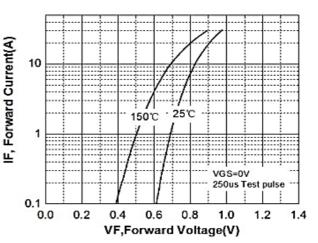
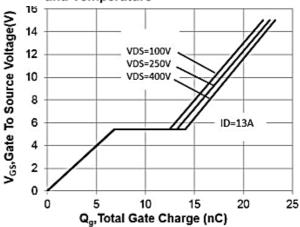
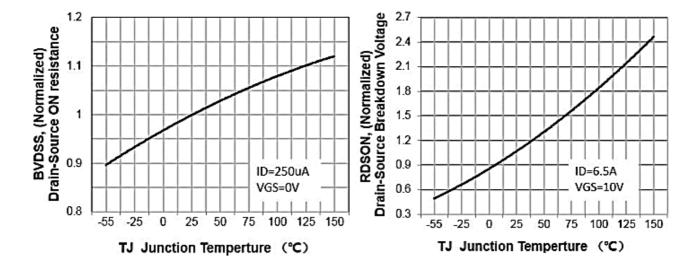


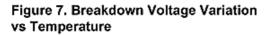
Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature











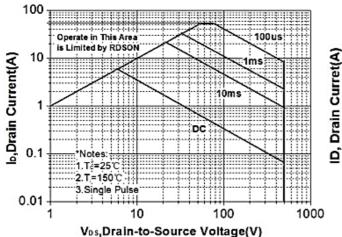
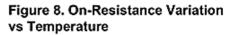


Figure 9. Maximum Safe Operating Area



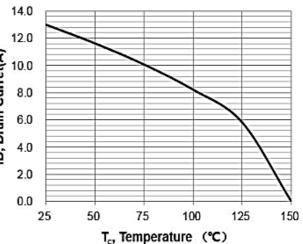


Figure 10. Maximum Drain Current vs Case Temperature

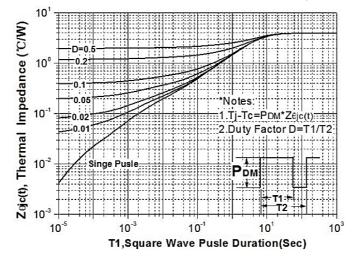
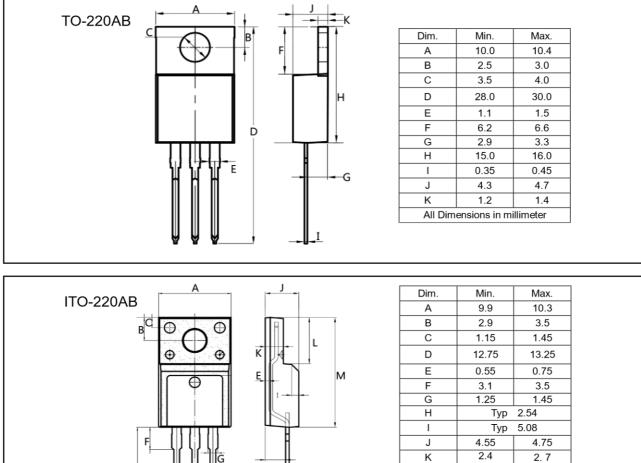
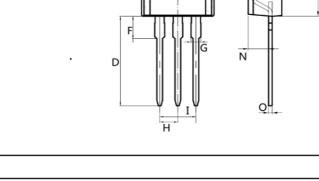


Figure 11. Transient Thermal Response Curve







В

I

D

+ F

TO-263

c

N	2.75	3.15	
0	0.45	0.60	
All Dimensions in millimeter			
Dim.	Min.	Max.	
A	10.0	10. 5	
В	7.25	7.75	
С	1.3	1.5	
D	0.55	0.75	
E	5.0	6.0	
F	1.4	1.6	
G	0.75	0.95	
Н	1.15	1.35	
I	Typ 2.54		
J	8.4	8.6	
K	4.4	4.6	
L	1.25	1.45	
М	0.02	0.1	
N	2.4	2.8	
0	0.25	0.45	

6.35

15.0

6.75

16.0

	L	1.25
	М	0.02
1N	N	24

L

Μ

Ο 0.35 0.45 All Dimensions in millimeter

М

ō



Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃ ±5 ℃	5sec±1sec
Pb-Free device	260 ℃ +0/-5 ℃	5sec±1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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