



Description

The XPX110N03FD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

$V_{DS} = 30V, I_D = 110A$

$R_{DS(ON)} = 3.6m\Omega$ (typ) @ $V_{GS} = 10V$

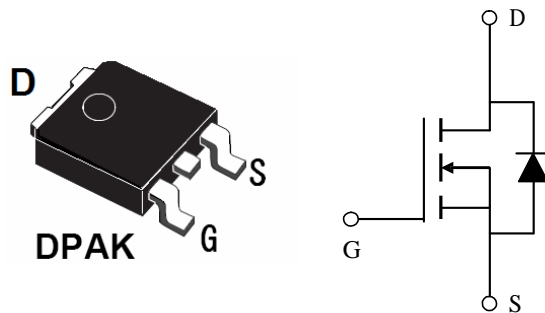
$R_{DS(ON)} = 5.5m\Omega$ (typ) @ $V_{GS} = 4.5V$

General Features

- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching



DUW U Y A U f] b [' U b X ' C f X Y f] b [' b z f a U] c b '

Product ID	Pack	Marking	Qty(PCS)
XPX110N03FD	TO-252-3L	XPX110N03FD XXX YYYY	2500

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	110	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	66	A
IDM	Pulsed Drain Current ^{note1}	400	A
EAS	Single Pulsed Avalanche Energy ^{note2}	163	mJ
IAS	Avalanche Current	19.5	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	68	W
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	62	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$)	25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.2	$^\circ C/W$
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175	$^\circ C$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	32	-	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.028	---	V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} =10V, I _D =30A	-	3.6	4.5	mΩ
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} =4.5V, I _D =20A	-	5.5	7.0	mΩ
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz	-	2018	-	pF
C _{oss}	Output Capacitance		-	326	-	pF
C _{rss}	Reverse Transfer Capacitance		-	282	-	pF
Q _g	Total Gate Charge	V _{DS} =15V, I _D =30A, V _{GS} =10V	-	45	-	nC
Q _{gs}	Gate-Source Charge		-	3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	15	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V, I _D =30A, R _{GEN} =3Ω, V _{GS} =10V	-	21	-	ns
t _r	Turn-on Rise Time		-	32	-	ns
t _{d(off)}	Turn-off Delay Time		-	59	-	ns
t _f	Turn-off Fall Time		-	34	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	90	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	360	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=100A/μs	-	15	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes:

- 1、 Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2、 The test condition is, V_{DD}=15V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=19.5A
- 3、 The data tested by pulsed Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%
- 4、 The power dissipation is limited by 150°C junction temperature

Typical Characteristics

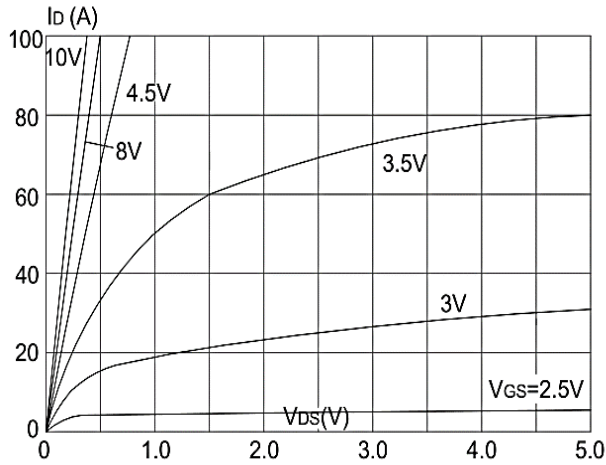


Figure 1: Output Characteristics

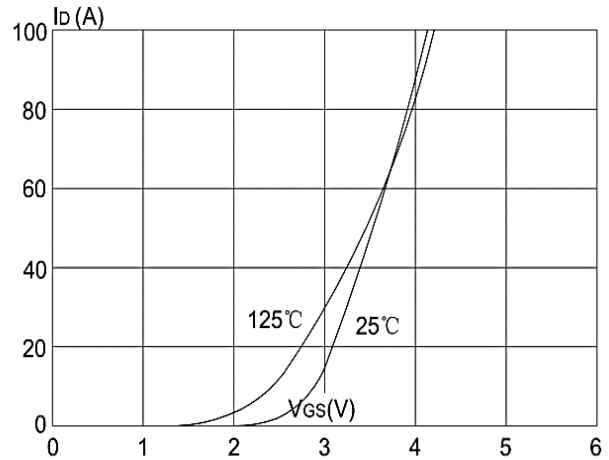


Figure 2: Typical Transfer Characteristics

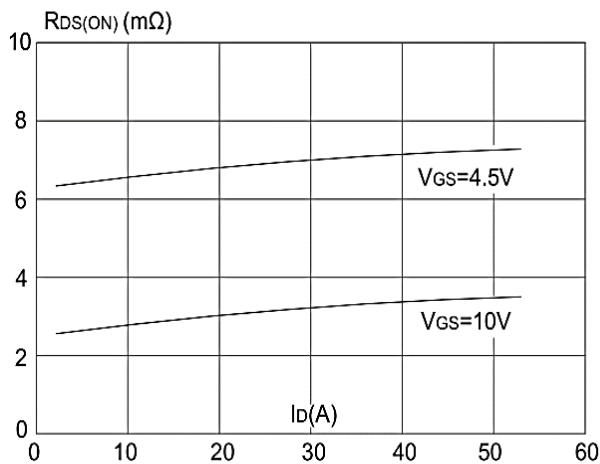


Figure 3: On-resistance vs. Drain Current

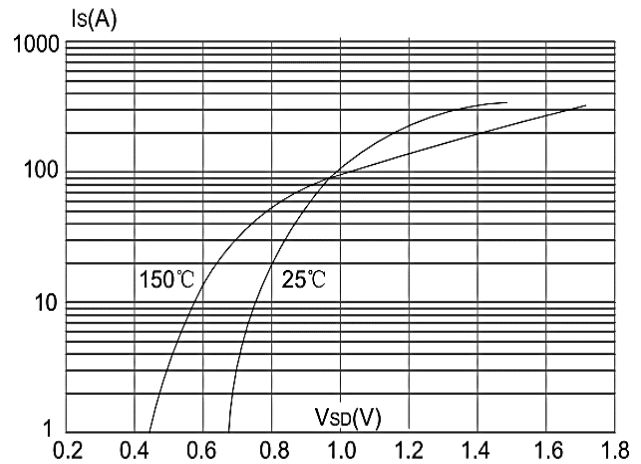


Figure 4: Body Diode Characteristics

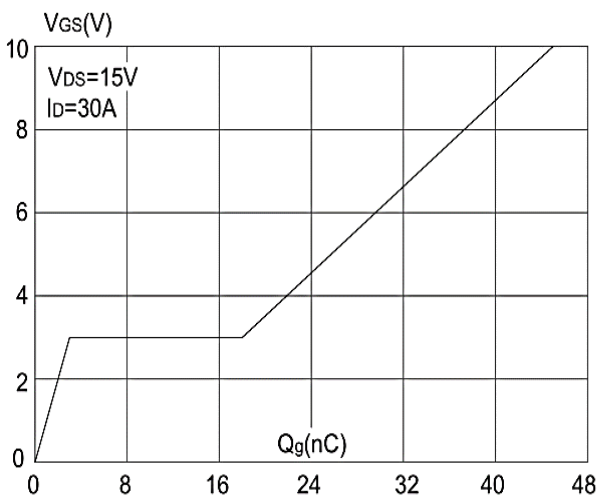


Figure 5: Gate Charge Characteristics

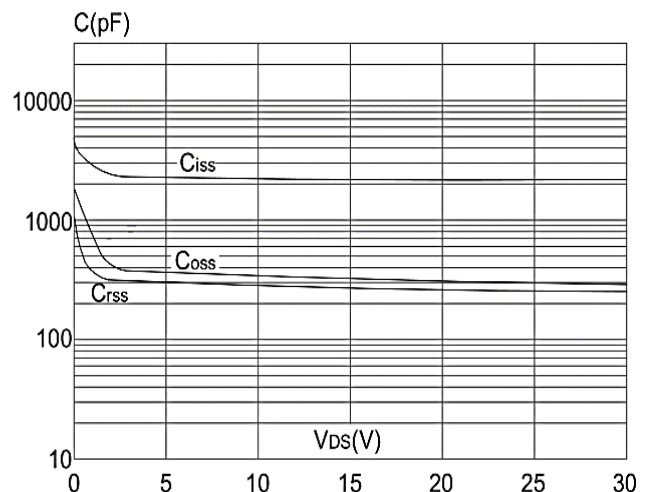


Figure 6: Capacitance Characteristics

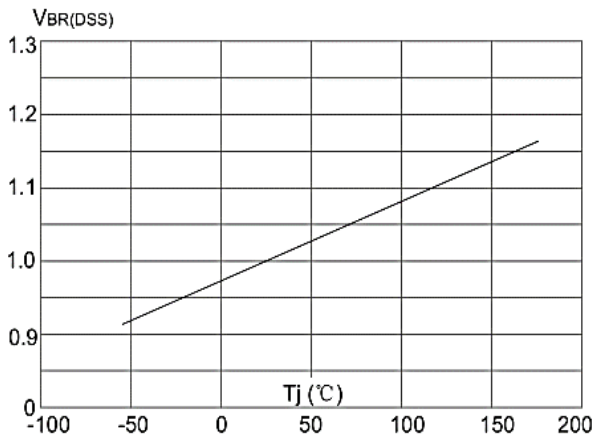


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

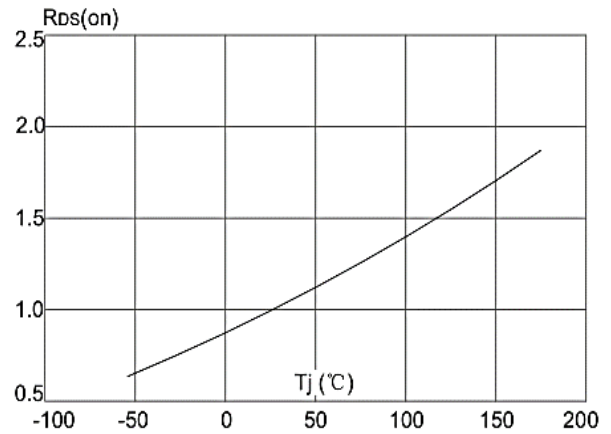


Figure 8: Normalized on Resistance vs. Junction Temperature

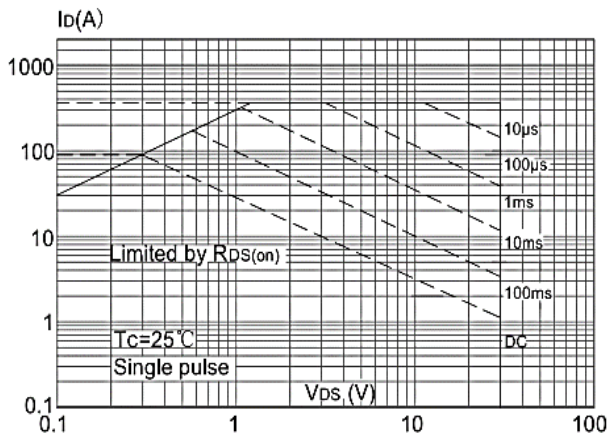


Figure 9: Maximum Safe Operating Area vs. Case Temperature

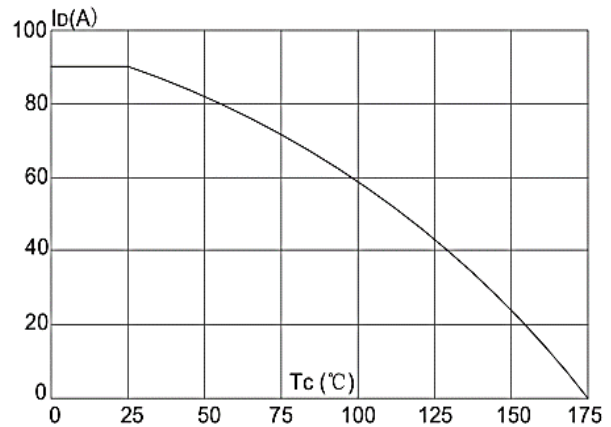


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

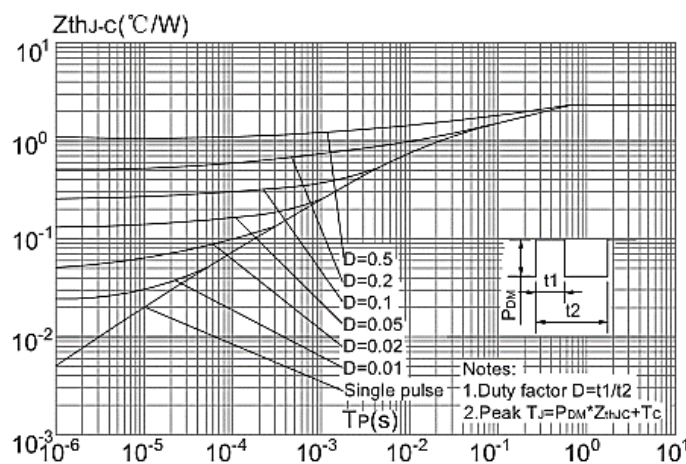
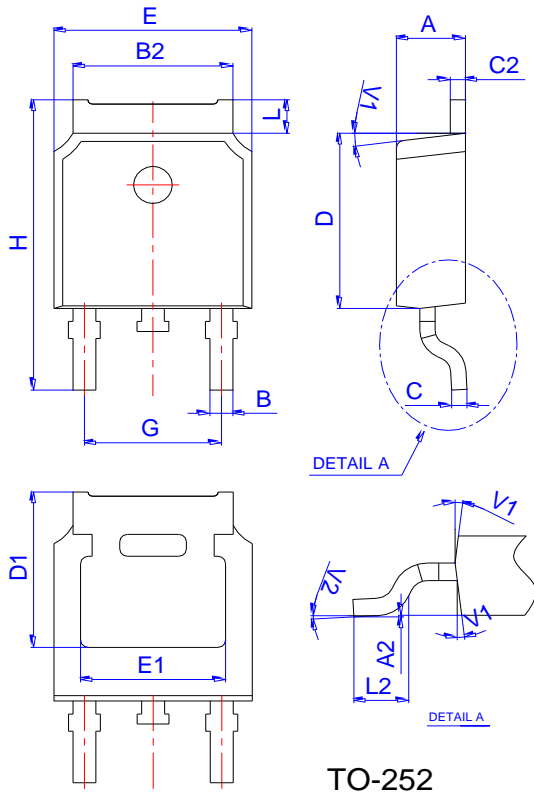


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

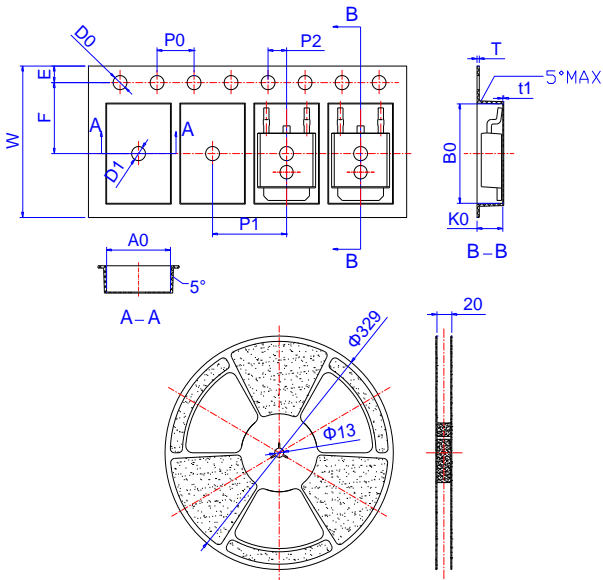
Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

TO-252

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec±1sec
Pb-Free device	260°C +0/-5°C	5sec±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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