100V N-ChannelEnhancement Mode Power MOSFET

Description

The XPX10N10XE uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

V_{DS} =100V,I_D =10A

$R_{DS(ON)}$=80mΩ (typ) @ V_{GS}=10V

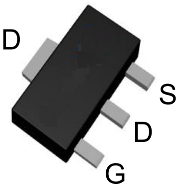
$R_{DS(ON)}$=95mΩ (typ) @ V_{GS}=4.5V

Application

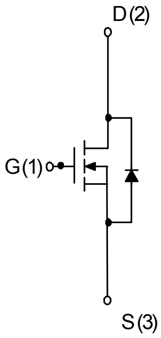
Lithium battery protection

Wireless impact

Mobile phone fast charging



Top View SOT-89



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX10N10XE	SOT89-3L	XPX10N10XE XXX YYYY	1000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	A
I_D@T_A=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	5.5	A
I_{DM}	Pulsed Drain Current[2]	15	A
P_D@T_A=25℃	Total Power Dissipation[3]	4.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{θJA}$	Thermal Resistance Junction-ambient [1]	88	℃/W
$R_{θJC}$	Thermal Resistance Junction-Case[1]	48	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100	---	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.122	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=3A	---	80	110	mΩ
		V_{GS}=4.5V , I_D=2A	---	95	125	mΩ
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	1.6	2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.84	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=100V , V_{GS}=0V , T_J=25℃	---	---	10	uA
		V_{DS}=100V , V_{GS}=0V , T_J=55℃	---	---	100	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=2A	---	10.2	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2.3	4.6	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=60V , V_{GS}=10V , I_D=2A	---	25.5	---	nC
Qgs	Gate-Source Charge		---	4.2	---	
Qgd	Gate-Drain Charge		---	4.3	---	
Td(on)	Turn-On Delay Time	V_{DD}=50V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	17.3	---	ns
T_r	Rise Time		---	2.8	---	
Td(off)	Turn-Off Delay Time		---	50	---	
T_f	Fall Time		---	2.8	---	
Ciss	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	698	---	pF
Coss	Output Capacitance		---	46	---	
Crss	Reverse Transfer Capacitance		---	32	---	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	2	A
ISM	Pulsed Source Current[2,4]		---	---	4	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150°C junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

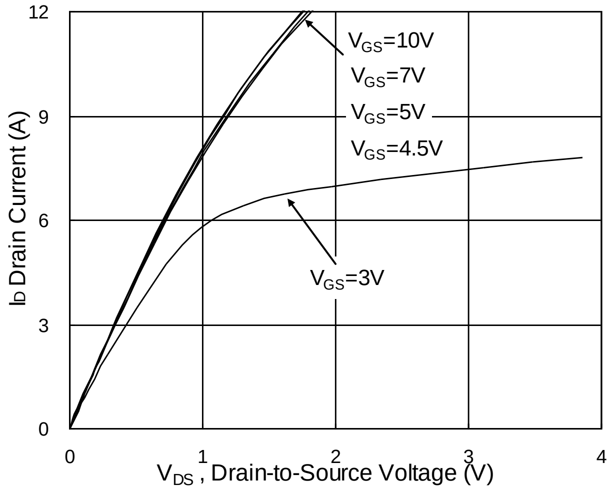


Fig.1 Typical Output Characteristics

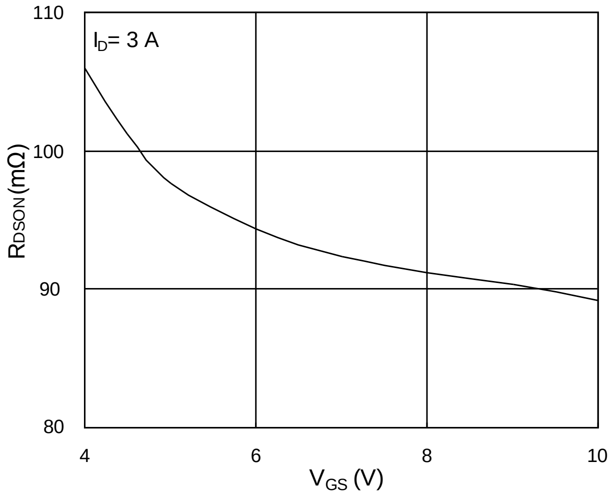


Fig.2 On-Resistance vs. Gate-Source

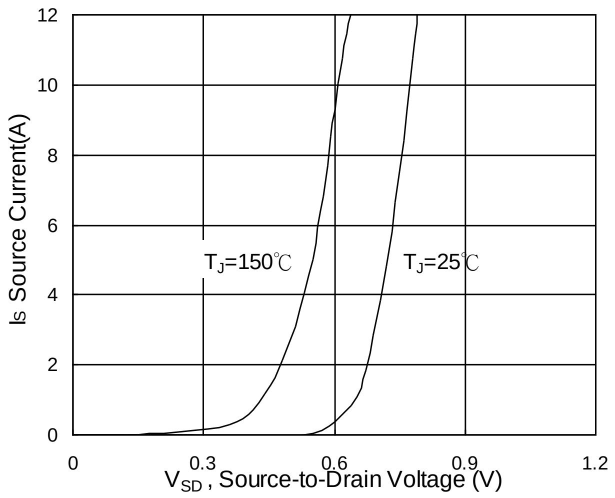


Fig.3 Forward Characteristics Of Reverse

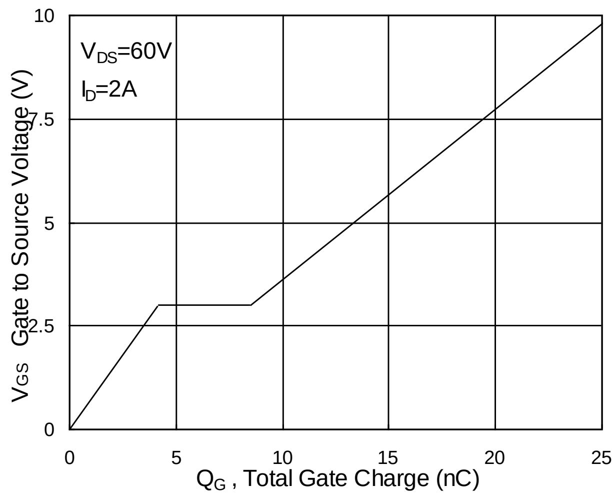


Fig.4 Gate-Charge Characteristics

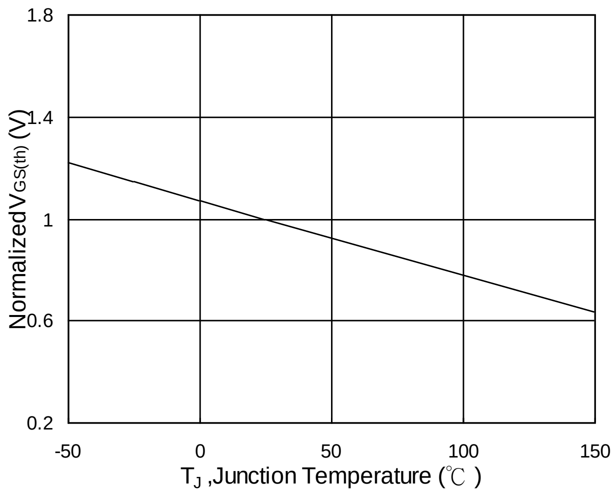


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

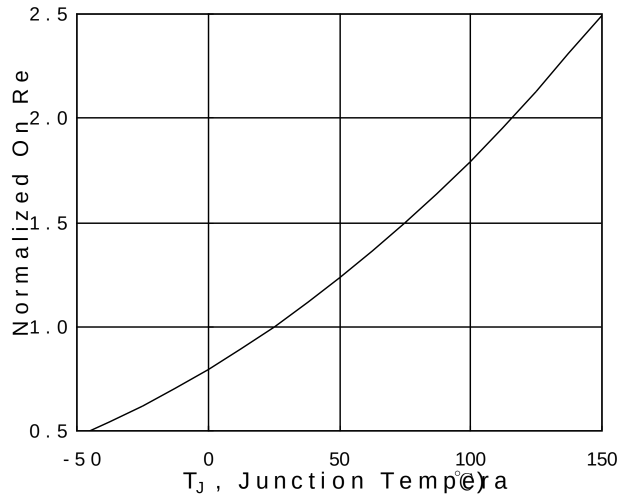


Fig.6 Normalized R_{DSON} vs. T_J

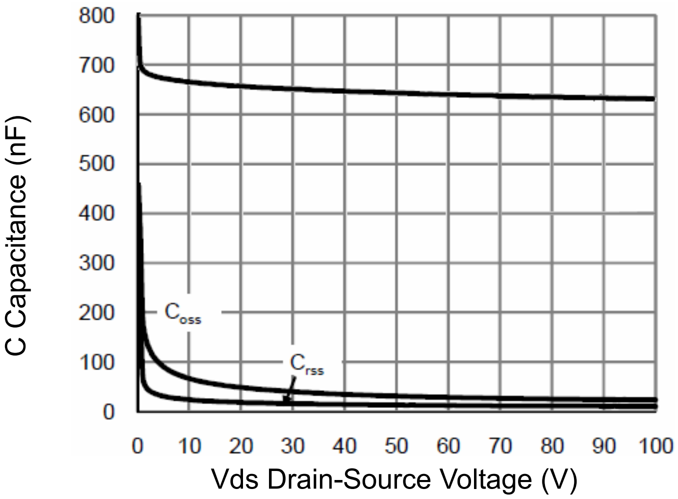


Figure 7 Capacitance vs Vds

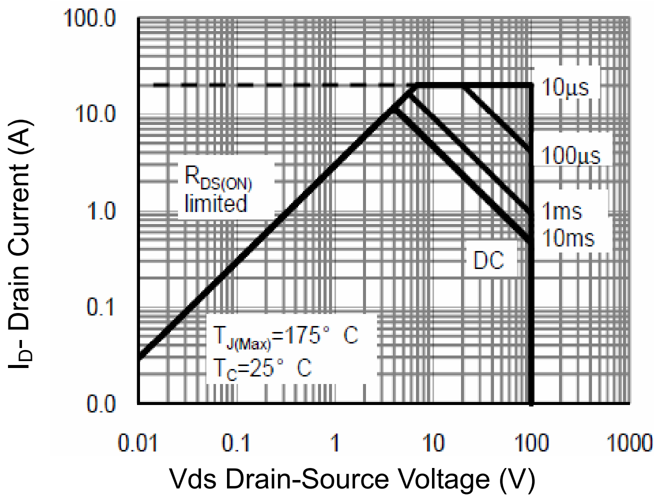


Figure 8 Safe Operation Area

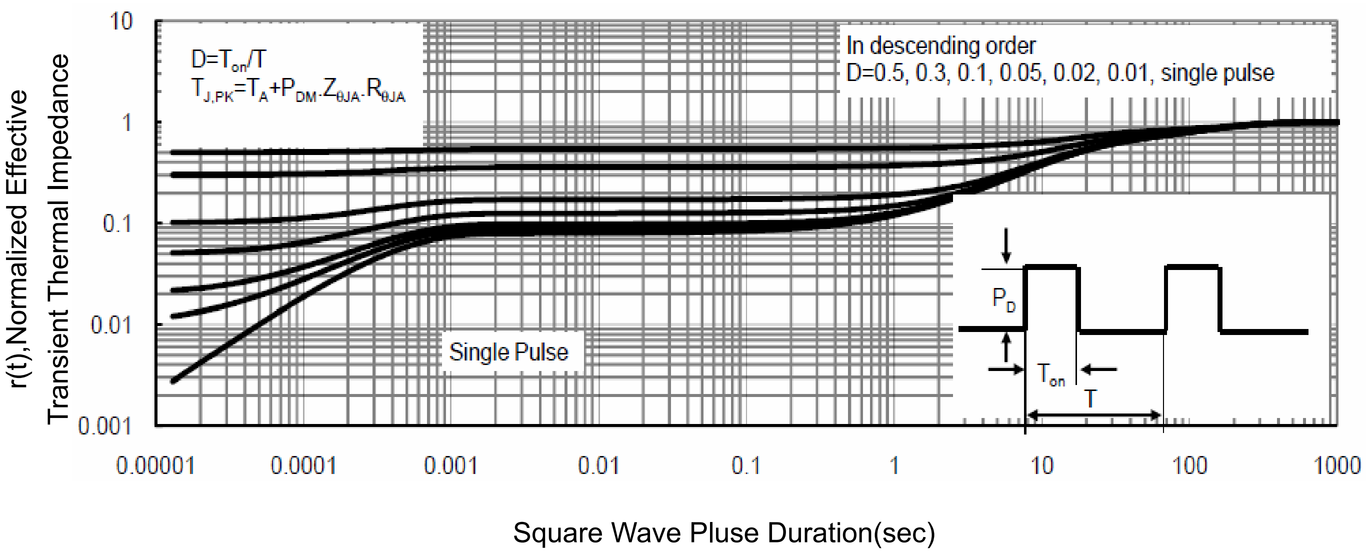
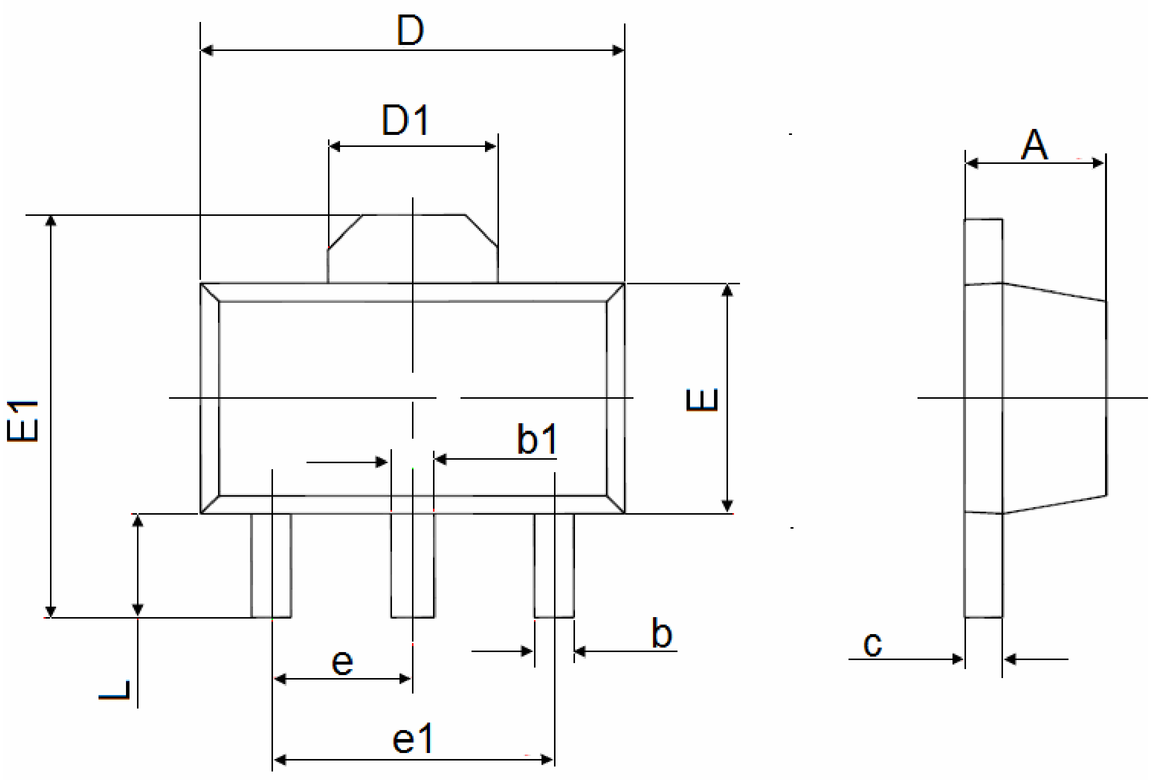


Figure 9 Normalized Maximum Transient Thermal Impedance

SOT-89-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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